COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

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AUGUST 1977

DESIGN DECISIONS ACHIEVE PRICE/PERFORMANCE BALANCE IN MID-RANGE MINICOMPUTERS

SOLVING MASS-PRODUCED ROM PROGRAMMING PROBLEMS WITH BASE REGISTERS

MULTIPLEXER SYSTEM REDUCES COST OF TERMINAL INTERFACING



Introducing

HP's first general-purpose Logic State Analyzer designed for both controllable production testing and field service... and it's low cost.

Until now, production line testing of digital equipment has meant complex test gear, large sums for computerized equipment or time-consuming manual checks . . . perhaps all three. In the field, it's been traditional test gear without the measurement capabilities of logic state analyzers.

Now, with the low-cost 1602A, HP offers a general-purpose, Logic State Analyzer that's easy to use in a number of plant or field applications. Manufacturing can use it in automatic functional test systems or in board-level and incoming inspection testing. And its ease of use, light weight and portability makes it a natural for field service applications, too.

The 1602A, priced at $1800*, is compatible with many logic systems having data rates to 10 MHz. It monitors, stores and displays activity on system buses or control lines (up to 64, 16-bit words on a single instrument) to verify proper system function.

It's portable, adaptable to automatic control, low cost and so easy to operate it's almost self teaching. It can boost your production-line testing throughput and field-service troubleshooting efficiency. Get all the details from your HP field engineer.

For manual production line testing and for field service troubleshooting, the 1602A keyboard lets you define testing and display parameters with just a few keystrokes. The LED display then lets you compare line or bus activity with test specifications.

For automatic systems, an HP-IB** option lets you do setups and evaluation using a computing controller. When used with HP's 9830A or 9825A controllers, programming is simple. An operator just presses a few special-function keys, and the HP-IB's "Learn Mode" does the rest.

Edge-connector probes speed setup. When test points are built into your system's boards or board extenders, the probes are simply plugged in. Time-consuming and error-prone probe connections can be eliminated.

This instrument minimizes chances of error two ways: Extensive messages tell the operator that the 1602A is being used properly. And internal diagnostics verify proper operation.





* Domestic U.S.A. price only.
** HP's implementation of IEEE Standard 488-1975.

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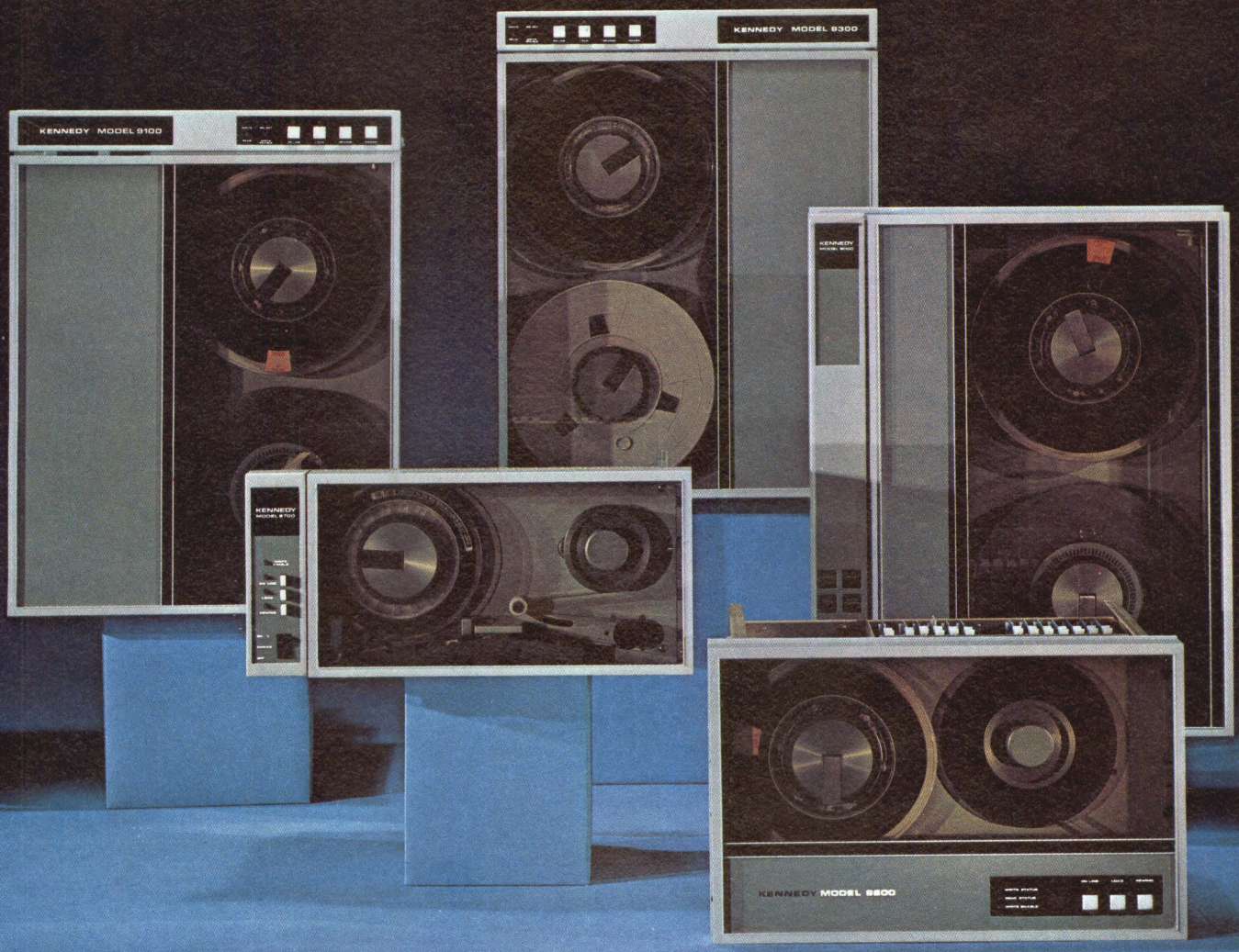
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CIRCLE 2 ON INQUIRY CARD



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Series 1 users can now add mag tape memory capability to their Series 1 (Models 3 or 5) installation! The new DATUM seven- or nine-track system permits recording densities of 200 bpi NRZ through 1600 bpi, phase-encoded. Speeds: from 12.5 ips through 125 ips. As many as four transports can be used.

Individually driven tape drive I/O ports. Read-after-write parity checking. Quartz-crystal-generated timing. Interfaces to industry-compatible drives.

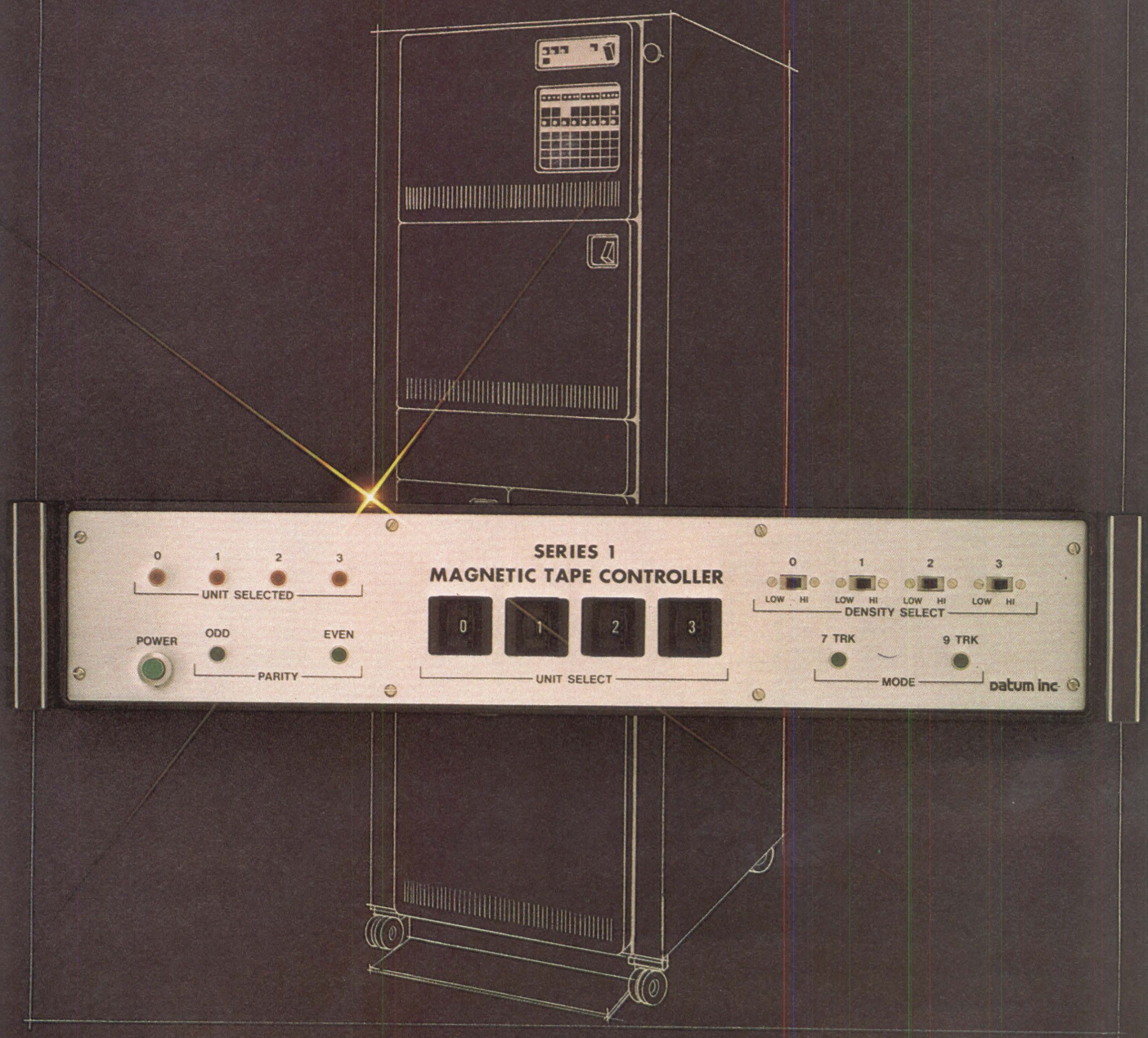
The system incorporates the new DATUM "Universal User's Adapter," a device that allows connection of external devices to the Input-Output bus of Models 3 or 5 of the IBM Series 1 computers. The Adapter operates in the "cycle -steal" mode while exchanging 16-bit words with the computer. With this Adapter, Series 1 users can tailor their system to their own exact requirements, even to the extent of interconnecting several computers.

Diagnostic and operational software is included with each system. Color-coordinated cabinets can be ordered. Service and installation are offered throughout the U.S. Deliveries are 90 to 120 days ARO.

CIRCLE 3 ON INQUIRY CARD

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Telex 68-5579

datum inc



THE MAGAZINE OF DIGITAL ELECTRONICS

COMPUTER DESIGN

AUGUST 1977 • VOLUME 16 • NUMBER 8

FEATURES

62 WESTERN ELECTRONIC SHOW AND CONVENTION
Advances, trends, and applications of electronic technology in microcomputers, LSI devices, automatic test equipment, semiconductor devices, and switching power supplies, among others, are explored during the in-depth technical sessions featured at WESCON/77

82 COMPCON 77 FALL
Commencing with tutorials emphasizing the design and applications of microprocessor systems, and outlining the emerging distributed processing technology, the IEEE Computer Society International Conference examines advances of technology in relation to micro, mini, and maxicomputers

87 DESIGN DECISIONS ACHIEVE PRICE/PERFORMANCE BALANCE IN MID-RANGE MINICOMPUTERS
by J. Craig Mudge
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99 SOLVING MASS-PRODUCED ROM PROGRAMMING PROBLEMS WITH BASE REGISTERS
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109 MULTIPLEXER SYSTEM REDUCES COST OF TERMINAL INTERFACING
by Austin Lesea and Nishan Urkumyan
Through careful determination of both hardware and software factors and their inter-relationships, a microprocessor-based multiplexer system is achieved that handles 32 EIA RS-232-C compatible terminals, and yet is compact, reliable, and cost-effective

116 FIFTH PRIZE—MICROPROCESSOR/MICROCOMPUTER APPLICATION CONTEST—ELECTRONIC DIET CONTROLLER
by Karen M. Moran
The need of many people to control their diets practically can be fulfilled with a microprocessor-based controller which allows monitoring of principal diet elements with clinic-like precision

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by K. Søe Højberg
A random priority arbiter with "n" parallel input channels is a solution to multiple requests and arbitration decisions for sharing of a common resource

150 DUAL SYSTEM DEVELOPS SOFTWARE FOR TWO INDEPENDENT MICROCOMPUTERS AT SAME TIME
Two programmers can develop software for different microprocessors simultaneously at approximately three-quarters the cost of two systems

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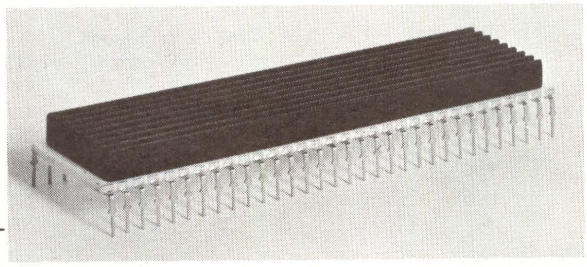
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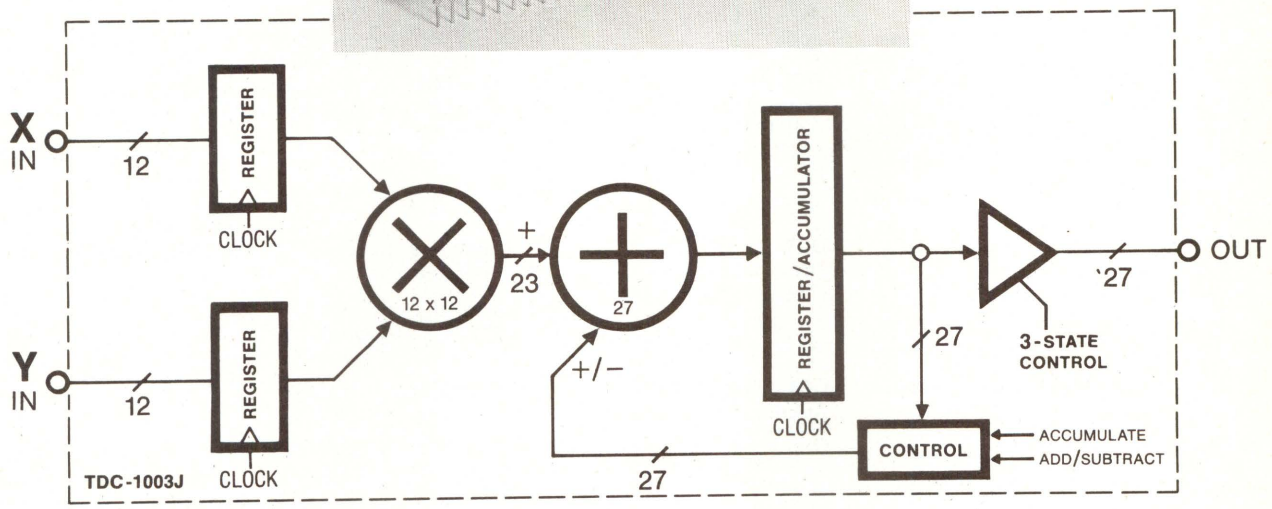
Editorial manuscripts should be addressed to Editor, Computer Design, 11 Goldsmith St., Littleton, MA 01460. For details on the preparation and submission of manuscripts, request a copy of the "Computer Design Author's Guide."

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CALENDAR

CONFERENCES

SEPT 6-9—Conf on Digital Processing of Signals in Communications, University of Technology, Loughborough, England. INFORMATION: Conference Secretariat, Institution of Electronic and Radio Engineers, 8-9 Bedford Sq, London WC1B 3RG, England

SEPT 6-9—COMPCON Fall (IEEE Computer Soc Internat'l Conf), Mayflower Hotel, Washington, DC. INFORMATION: COMPCON Fall '77, PO Box 639, Silver Spring, MD 20901. Tel: (301) 439-7007

SEPT 6-10—INELTEC '77, U.S. Computer and Peripheral Catalog Exhibition, Basel, Switzerland. INFORMATION: U.S. Dept of Commerce, Domestic and Internat'l Business Administration, Catalog Exhibition Section, Washington, DC 20230. Tel: (202) 377-3973

SEPT 7; OCT 4; and OCT 27—Invitational Computer Conf, Boston Marriott, Newton, Mass; Radisson South, Minneapolis, Minn; and Cabana Hyatt House, Palo Alto, Calif. INFORMATION: B. J. Johnson & Associates, 2503 Eastbluff Dr, Suite 203, Newport Beach, CA 92660. Tel: (714) 644-6037

SEPT 19-21—WESCON (Western Electronic Show and Convention), San Francisco, Calif. INFORMATION: William C. Weber Jr, Gen'l Mgr, WESCON, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 1-800-421-6816

SEPT 25-28—EASCON-77 (Electronics and Aerospace Systems Conf), Sheraton Nat'l Hotel, Arlington, Va. INFORMATION: Wayne Shufelt, EASCON-77 Publicity Chm, Sperry Univac, 2121 Wisconsin Ave, NW, Washington, DC 20007. Tel: (202) 338-8500

SEPT 26-28—Distributed Computer Control Systems Internat'l, University of Aston, Birmingham, England. INFORMATION: IEE, Savoy Place, London WC2R OBL, England

SEPT 26-29—13th Electrical/Electronics Insulation Conf, Palmer House, Chicago, Ill. INFORMATION: R. E. Pritchard, 1717 Howard St, Evanston, IL 60202. Tel: (312) 491-1662

SEPT 27-29—Military Electronics Defense Expo 77, Wiesbaden, West Germany. INFORMATION: Joseph Maurer, Industrial & Scientific Conf Mgmt, Inc, 222 W Adams St, Chicago, IL 60606. Tel: (312) 263-4866

OCT 3-5—Sym on Computer Application in Medical Care, Washington, DC. INFORMATION: IEEE Computer Society, Exec Secretary, PO Box 639, Silver Spring, MD 20901. Tel: (301) 439-7007

OCT 3-6—EUROMICRO Sym, Amsterdam, The Netherlands. INFORMATION: Ted Holtwijk, Philips Elcoma, Bldg BAE 2, NL-Eindhoven, The Netherlands

OCT 4-6—NEPCON Central '77 (Nat'l Electronics Packaging and Production Conf), O'Hare Internat'l Trade and Exposition Ctr and Hyatt Regency O'Hare Hotel, Rosemont, Ill. INFORMATION: Industrial & Scientific Conf Mgmt, Inc, 222 W Adams St, Chicago, IL 60606. Tel: (312) 263-4866

OCT 6-8—3rd Internat'l Conf on Very Large Data Bases, Tokyo, Japan. INFORMATION: James Gabbert, MIT Sloan School, 50 Memorial Dr, Rm E53-330, Cambridge, MA 02139

OCT 6-12—Stockholm Internat'l Technical Fair, Stockholm, Sweden. INFORMATION: Radley Communications Ltd, 509 Madison Ave, New York, NY 10022. Tel: (212) 838-9215

OCT 9-15—INTELCOM '77 (Internat'l Telecommunications Exposition), Atlanta, Ga. INFORMATION: Barbara Coffin, Promotion Mgr, Horizon House Internat'l, 610 Washington St, Dedham, MA 02026. Tel: 1-800-225-9977, (617) 326-8220

OCT 10-13—10th Conv of Electrical and Electronic Engineers in Israel, Tel Aviv. INFORMATION: Daphna Knassim Ltd, 444 Madison Ave, New York, NY 10022. Tel: (212) 688-7072

OCT 17-20—ISA/77 (Instrument Society of America Conf & Exhibit), Internat'l Conv Ctr, Niagara Falls, NY. INFORMATION: Instrument Society of America, 400 Stanwix St, Pittsburgh, PA 15222. Tel: (412) 281-3171

OCT 18-20—Internat'l Conf on Modeling Semiconductor Devices, Lausanne, Switzerland. INFORMATION: Secrétariat des Journées d'électronique, Dept d'électricité-EPFL, 16 chemin de Bellerive, CH-1007 Lausanne, Switzerland

OCT 19-20—10th Annual Electrical Connector Sym, Cherry Hill, NJ. INFORMATION: Electronic Connector Study Group, Inc, PO Box 1428, Camden, NJ 08101. Tel: (609) 424-4014

OCT 25-27—Semiconductor Test Sym, Cherry Hill, NJ. INFORMATION: Mrs. R. J. Sunderland, Secretary and Registrar, Test Symposium Committee, PO Box 2340, Cherry Hill, NJ 08034. Tel: (609) 424-2400

OCT 28—Society for Information Display (SID) One-Day Technical Conf, Sheraton Inn/Airport, San Diego, Calif. INFORMATION: Dan Heflinger, DatagraphiX, Inc, PO Box 82449, San Diego, CA 92138. Tel: (714) 291-9960

OCT 31-NOV 2—AIAA/IEEE/NASA Computers in Aerospace, Hyatt House Hotel, Los Angeles, Calif. INFORMATION: Hugh Harrington, Dept E411, McDonnell Douglas Astronautics, PO Box 516, St Louis, MO 63166. Tel: (314) 232-9102

NOV 2-4—AUTOTESTCON '77 (IEEE Internat'l Automatic Testing Conf), Dunfey's Resort, Hyannis, Mass. INFORMATION: Eugene B. Galton, Gen'l Chm, AUTOTESTCON 77, RCA Corp, PO Box 588, Burlington, MA 01803. Tel: (617) 272-4000

NOV 7-11—Electronic Components 77, U.S. Trade Ctr, London, England. INFORMATION: Robert Connan, Office of Internat'l Mktg, U.S. Dept of Commerce, Washington, DC 20230. Tel: (202) 377-3465

NOV 8-10—Compec UK '77 (Computer Peripherals Exhibition), Wembley Centre, London, England. INFORMATION: Iliffe Promotions Ltd, Dorset House, Stamford St, London SE1-9LU, England

NOV 8-10—MIDCON, O'Hare Conv Ctr and Hyatt Regency Hotel, Chicago, Ill. INFORMATION: W. C. Weber Jr, IEEE, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: (213) 772-2965

NOV 8-11—COMPSAC '77 (IEEE Computer Soc Software & Applications Conf), Sheraton-O'Hare Motor Hotel, Chicago, Ill. INFORMATION: Prof Stephen S. Yau, Dept of Computer Science, Northwestern U, Evanston, IL 60201. Tel: (312) 492-3641

SEMINARS

AUG 22-26—Microcontrollers 6800-8080, Rowntowner Motel, Rochester, NY. INFORMATION: InfoScope Inc, PO Box 681, E Brunswick, NJ 08816. Tel: (201) 238-2220

SEPT 19-21—Minicomputers, U of Chicago, Chicago, Ill. INFORMATION: William A. Kulok, New York Mgmt Ctr, 360 Lexington Ave, New York, NY 10017. Tel: (212) 953-7262

SHORT COURSES

SEPT 7-9—Computer Programming for the Non-Programmer; SEPT 12-16—Telecommunications Policy Problems; SEPT 14-16—Software Design for Data Communication Systems; and SEPT 19-23—Modern Data Communications, George Washington U, Washington, DC. INFORMATION: Director, Continuing Engineering Education, George Washington U, Washington, DC 20052. Tel: (202) 676-6106, 1-800-424-9773

SEPT 12-16—Bubble Domain Technology, UCLA, Los Angeles, Calif. INFORMATION: Continuing Education in Engineering and Mathematics, Short Courses, 6266 Boelter Hall, UCLA Extension, Los Angeles, CA 90024. Tel: (213) 825-1047

SEPT 26-30—Mini/Microcomputer Systems, Milwaukee, Wis. INFORMATION: John T. Snedeker, Dept of Engineering, U of Wisconsin-Ext, Civic Ctr Campus, 929 N 6th St, Milwaukee, WI 53203. Tel: (414) 244-4193

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- [x] MC6800P — Microprocessor
- [ ] MC6800CP — Microprocessor
- [ ] MC6800MTL — Microprocessor
- [x] MC6800ML — Microprocessor
- [x] MC68A00P — Microprocessor
- [x] MC68B00P — Microprocessor
- [x] MC68A00L — Microprocessor
- [x] MC68B00L — Microprocessor
- [x] MC6802P — Microprocessor + RAM & Clock
- [ ] MC6802CP — Microprocessor + RAM & Clock
- [x] MC6802L — Microprocessor + RAM & Clock
- [ ] MC6802CL — Microprocessor + RAM & Clock
- [x] MCM6810P — Byte-Organized RAM
- [ ] MCM6810CP — Byte-Organized RAM
- [x] MCM68A10P — Byte-Organized RAM
- [x] MCM68A10L — Byte-Organized RAM
- [x] MCM68B10P — Byte-Organized RAM
- [x] MCM68B10L — Byte-Organized RAM
- [ ] MCM6810MTL — Byte-Organized RAM
- [ ] MCM6810ML — Byte-Organized RAM
- [x] MC6821P — Peripheral Interface Adapter
- [ ] MC6821CP — Peripheral Interface Adapter
- [x] MC6821L — Peripheral Interface Adapter
- [ ] MC6821CL — Peripheral Interface Adapter
- [ ] MC68A21P — Peripheral Interface Adapter
- [ ] MC68A21L — Peripheral Interface Adapter
- [ ] MC68B21P — Peripheral Interface Adapter
- [ ] MC68B21L — Peripheral Interface Adapter
- [ ] MC6821MTL — Peripheral Interface Adapter
- [ ] MC6821ML — Peripheral Interface Adapter
- [ ] MC6840P — Programmable Timer
- [ ] MC6840CP — Programmable Timer
- [ ] MC6840L — Programmable Timer
- [ ] MC6840CL — Programmable Timer
- [ ] MC68A40P — Programmable Timer
- [ ] MC68A40L — Programmable Timer
- [ ] MC68B40P — Programmable Timer
- [ ] MC68B40L — Programmable Timer
- [ ] MC6840MTL — Programmable Timer
- [ ] MC6843P — Floppy Disk Controller
- [ ] MC6843L — Floppy Disk Controller
- [ ] MC6844P — DMA Controller (1.0 MHz)
- [ ] MC6844L — DMA Controller
- [ ] MC6845P — CRT Controller
- [ ] MC6845L — CRT Controller
- [ ] MC6846P — MC6802 Combo
- [ ] MC6846CP — MC6802 Combo
- [ ] MC6846L — MC6802 Combo
- [ ] MC6846CL — MC6802 Combo
- [x] MC6850P — Asynch. Comm. Interface Adapter
- [ ] MC6850CP — Asynch. Comm. Interface Adapter
- [x] MC68A50P — Asynch. Comm. Interface Adapter
- [x] MC68A50L — Asynch. Comm. Interface Adapter
- [x] MC68B50P — Asynch. Comm. Interface Adapter
- [x] MC68B50L — Asynch. Comm. Interface Adapter
- [ ] MC6850MTL — Asynch. Comm. Interface Adapter
- [ ] MC6850ML — Asynch. Comm. Interface Adapter
- [x] MC6852P — Synchronous Serial Data Adapter
- [ ] MC6852CP — Synchronous Serial Data Adapter
- [ ] MC68A52P — Synchronous Serial Data Adapter
- [ ] MC68A52L — Synchronous Serial Data Adapter
- [ ] MC6852MTL — Synchronous Serial Data Adapter
- [ ] MC6854P — Advanced Data Link Controller
- [ ] MC6854CP — Advanced Data Link Controller
- [ ] MC6854L — Advanced Data Link Controller
- [ ] MC6854CL — Advanced Data Link Controller
- [ ] MC68A54P — Advanced Data Link Controller
- [ ] MC68A54L — Advanced Data Link Controller
- [ ] MC68B54P — Advanced Data Link Controller
- [ ] MC68B54L — Advanced Data Link Controller
- [ ] MC6854MTL — Advanced Data Link Controller
- [x] MC6860P — 0—600 bps Modem
- [x] MC6862P — 2400 bps Modulator
- [ ] MC6875P — Clock Oscillator/Driver—
- [ ] MC6875L — Clock Oscillator/Driver—
- [ ] MC68488P — General-Purpose Interface Adapter
- [ ] MC68488CP — General-Purpose Interface Adapter
- [ ] MC68488L — General-Purpose Interface Adapter
- [ ] MC68488CL — General-Purpose Interface Adapter
- [ ] MC68A488P — General-Purpose Interface Adapter
- [ ] MC68A488L — General-Purpose Interface Adapter
- [ ] MC68B488P — General-Purpose Interface Adapter
- [ ] MC68B488L — General-Purpose Interface Adapter
- [ ] MC68488MTL — General-Purpose Interface Adapter
- [x] MCM6830P — 1K ROM
- [ ] MCM6830CL — 1K ROM
- [ ] MCM68A30P — 1K ROM
- [ ] MCM68A30L — 1K ROM
- [ ] MCM68B30P — 1K ROM
- [ ] MCM68B30L — 1K ROM
- [x] MCM68308P — 8K ROM
- [x] MCM68308L — 8K ROM
- [ ] MCM68308CL — 8K ROM
- [ ] MCM68A308P — 8K ROM
- [ ] MCM68A308L — 8K ROM
- [ ] MCM68316AP — 16K ROM
- [ ] MCM68316AL — 16K ROM
- [x] MCM68316EP — 16K ROM
- [x] MCM68316EL — 16K ROM
- [ ] MCM68A316EL — 16K ROM
- [x] MCM68708L — 8K EPROM
- [x] MCM68A708L — 8K EPROM

2nd Quarter, 1978

- [ ] MC6801 — Microprocessor

3rd Quarter, 1978

- [ ] MC6809 — Microprocessor

☐ Introduced
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Frequency Range
MC68XX = 1.0 MHz
MC68AXX = 1.5 MHz
MC68BXX = 2.0 MHz

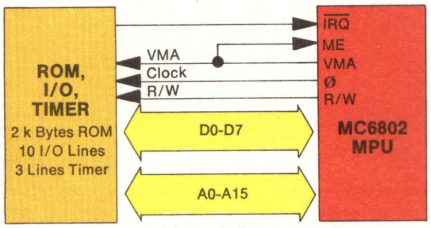
Temperature
MC68XX = 0°C to +70°C
MC68XXC = -40°C to +85°C
MC68XXMT = -55°C to +125°C
MC68XXM = MIL-883

Package
MC68XXP = Plastic
MC68XXL = Ceramic

Pin-Out Variations
Suffix A, Suffix E

computer commitment you've seen.

Here's #37 in 1977: the MC6802 for cost-effective two-chip systems.

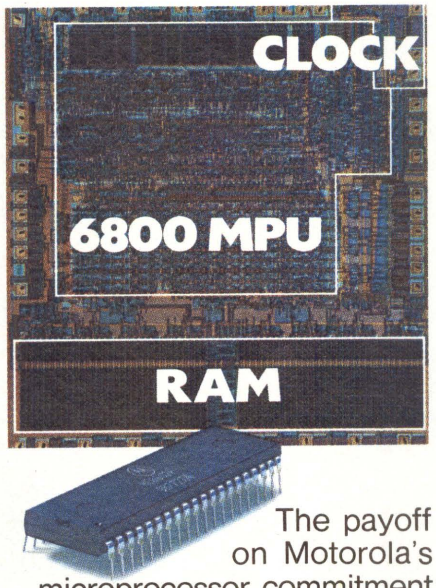


MC6802 Two-chip minimum system

Here, on a single chip, is a complete MC6800 microprocessor, plus a clock and 128 bytes of RAM. The first 32 bytes of that RAM can be held in a low-power mode for memory retention during power-down situations. Add the soon-to-be available MC6846 ROM-I/O-Timer combo circuit, and you have a complete, cost-effective minimum microcomputer system.

The glory of it all is total compatibility: not just software compatibility, but software and hardware compatibility plus bus compatibility. The powerful MC6802 instruction set is identical to the MC6800. Total compatibility with the M6800 Family; there's no need for extra training, and no need for different or additional hardware or software. It also means the MC6802 is easily expanded to 65K words.

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CIRCLE 6 ON INQUIRY CARD

LETTERS TO THE EDITOR

To the Editor:

Prosser and Winkel ("Mixed Logic Leads to Maximum Clarity with Minimum Hardware," *Computer Design*, May 1977) have made an incorrect generalization when they conclude that no textbooks emphasize the mixed logic approach to logical design. Several texts, including *The Design of Digital Systems*, by Peatman (McGraw-Hill, 1972) and *Fundamentals of Digital Systems Design* by Rhyne (Prentice-Hall, 1973), introduce this technique and make extensive use of its capabilities as a combinational design tool. The latter text has even been in use within the Electrical Engineering Department at the University of Wyoming, Winkel's "home base," for the past several years.

The real problem with the use of mixed logic (or the "polarity indicator system" as the current ANSI-IEEE standard calls it) is the use of the circle or bubble to represent the low-TRUE condition. This has been popularized in industrial practice, even though it uses the same symbol to represent *both* logical inversion and negative-TRUE polarity assignment. In an attempt to clarify this situation, many different approaches to denoting polarity have been introduced, including the H/L trailing letter espoused by Prosser and Winkel, and the use of plus and minus signs carried along with each logical symbol name. The ANSI-IEEE standard currently in effect adds a new symbol, a triangular wedge, that indicates when input or output signals are negative-TRUE. Widespread acceptance of this symbol is yet to be seen.

Unfortunately, the approach to logic design that is recommended in the ANSI-IEEE standard insists upon the use of either a polarity based system (wherein the logical NOT function is never used) or the use of a fixed-polarity system. As Prosser, Winkel, and several others have pointed out, the combined use of both the NOT *and* changes in polarity results in a most straightforward methodology for digital systems design.

Tom Rhyne
Texas A&M University
College Station, Tex

The Authors Reply:

Tom Rhyne's textbook does indeed espouse mixed logic design. Rhyne emphasizes the vital distinction between logic level and voltage level; and although we do not enjoy his choice of notation, we are delighted to have this use of mixed logic pointed out to us. The Peatman textbook does not use mixed logic, instead using the positive-true convention (p 70 and subsequent examples). Peatman's small circle represents a logic inversion, rather than a voltage convention. As we have seen, this leads to unnecessary complications.

Franklin Prosser
David Winkel
Indiana University
Bloomington, Ind

To the Editor:

I commend your journal and authors Prosser and Winkel on the recent article concerning mixed logic.[1] I have been applying the logic concepts outlined in that article in my designs for over 15 years. I also teach a course in logic design and include these concepts in my lectures.

Computer Design published two articles on mixed logic in 1970-1971.[2,3] I thought that those articles presented a very ambiguous approach to the problem and stated some of my ideas in a letter to the editor.[4] Several other letters on the subject followed, and I received several personal letters from design engineers that expressed agreement with my position.

Now, seven years later, a problem still exists concerning the practical and logical concepts of using mixed logic in logic design. Prosser and Winkel have done an excellent job of stating the problems and demonstrating the clarity obtained in *correct* mixed logic designs. The problem still exists because engineering texts gloss over these mixed logic concepts, if they mention them at all, and do not leave the student with a clear understanding of what it's all about. I too, like Prosser and Winkel, hope that experienced and new design engineers will adopt these concepts that lead to superior designs.

References

1. F. Prosser and D. Winkel, "Mixed Logic Leads to Maximum Clarity with Minimum Hardware," *Computer Design*, May 1977, pp 111-117
2. V. Ellis, "Positive and Negative Logic," *Computer Design*, Sept 1970, pp 79-84
3. P. M. Kintner, "Mixed Logic: A Tool for Design Simplification," *Computer Design*, Aug 1971, pp 55-60
4. J. S. Byrd, "Letters to the Editor," *Computer Design*, Mar 1972, p 10

J. S. Byrd
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Aiken, SC

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CIRCLE 7 ON INQUIRY CARD

by John E. Buckley
Telecommunications Management Corp
Cornwells Heights, Pa.

Computerized Voice Network Control

Recent "Communication Channel" columns have discussed the nature and application of the revised AT&T tariffs, particularly the Wide Area Telecommunications Service. These tariffs define communications services that are widely used for both data and voice communications requirements. Major changes with respect to both rates and structure automatically impact a wide spectrum of information system users and applications. Unless these changes are quickly assessed with respect to each individual environment, many systems unknowingly and unnecessarily incur higher communications costs.

The largest segment of communications users comprises business administrative voice applications. Data communications activities are embedded in a number of such applications. As discussed last month, the trend of these newer communications service tariffs is to provide the user with less visibility into the source of this communication cost as well as with fewer alternatives to maximize the value returned on his monthly communications investment. Communications system management unfortunately is evolving toward more estimate-derived rather than factually-based decisions.

Communications common carriers (ie, telephone companies) in attempting to minimize their billing costs are also reducing usage visibility and restricting network design alternatives. An additional factor that must be considered in light of these continuing tariff trends is the economy potentially available from various private line tariffs as alternatives to the switched network tariffs such as the Wide Area Telecommunications Service (WATS) Tariff (FCC Tariff No 259).

Communications system designers and managers have typically been very selective in their application of private or leased lines, such as foreign exchange service or tie-lines, due to the highly limited permissible calling area. A foreign exchange service to a remote city must be limited to that city's metropolitan area and perhaps selective surburban areas in order to realize anticipated calling cost savings and to avoid toll charges generated from the foreign exchange line. Unfortunately, the acceptable calling area for such a foreign exchange service is not easily identified. Permitted calling area of a WATS line can be defined with respect to area codes which comprise part of the called number. A permitted "local" calling area for a foreign exchange service would typically consist of a few hundred randomized telephone company central office designations or an extensive list of city and town names that are not necessarily known to the call originator. In such an environment, personnel procedural adherence can reasonably be expected to be quite low. The result, therefore, has been the limited use of such foreign exchange services on either a local or national basis.

Under the revised WATS rates the cost per minute for a band 1 WATS call would be approximately $0.276 assuming the average monthly line utilization of 40 hours. A foreign exchange service to a major city in that band (New York to Philadelphia) would cost approximately $0.063/min for a foreign exchange service carrying the same traffic volume. While such a dramatic cost savings should generate a high demand for such private line services, the operational complexity tends to negate any such potential value.

Both of these management concerns of increasing visibility and the application of alternative network services has significantly stimulated the demand for computerized communications systems. The access, control, and monitoring of these various communications network services must be under the direction and supervision of a computerized switching system. These computerized branch exchanges (CBX) have rapidly established all the traditional nonprogrammable voice-grade communications switching systems as obsolete.

"Computerized PBX Systems" ("Communication Channel," *Computer Design*, May 1976, pp 14, 19) discussed the concept of this blending of computer and telephone system technologies. Of the CBX examples discussed in that column, the Rolm CBX system and the Western Electric Dimension system have emerged as the leading computerized telephone systems by virtue of installed population. The Dimension system is provided exclusively through the AT&T operating telephone companies, on a state-tariffed monthly rental basis, while the Rolm CBX system is available as an interconnect system. As such, the functions available with a Dimension system may vary according to the individual state's communication tariff provisions; all Rolm CBX systems provide the same capabilities. For purposes of illustration, therefore, the role of a computerized telephone system in this discussion will relate to the Rolm CBX system.

Increased Visibility

In order to properly manage any dynamic environment, the means must be available to constantly measure the

activities and events within that environment. This premise, coupled with the magnitude of costs associated with a communications network, further emphasizes the necessity for such visibility. In addition, that visibility must be timely. It would be totally academic to analyze the communications activity of six months ago in order to formulate communications network decisions for next month. Particularly during periods of unusual change, such as a rate increase or reconfiguration of a communications network, management must be able to rapidly ascertain any value impact and quickly adjust accordingly. This can only be achieved by a call recording environment under total control of the network's communications manager.

Many communications facilities with a major monthly expense often have no way of monitoring or tracking their actual usage and hence the value returned from that monthly investment. Such facilities would comprise local calling, In-WATS, tie-lines, and foreign exchange services. Actual calling usage data for toll calling and outward-WATS service can typically be obtained from the associated telephone companies for an additional charge, and with a significant delay from the time of the call to the time the data are available.

A computerized communications system will record all calling activity by individual calls for every incoming as well as outgoing call, regardless of the actual communications facility utilized. This basic information must be coupled with the call destination identification, and for outgoing calls, the call origination identification. Selective compilation of this CBX-produced usage data enables the manager to properly assess the present value of the communications network and accurately identify network modifications that would return an even greater value.

Many times the course of action required to realize an improved value rate of return includes significant calling procedural modifications. These procedures usually involve a large, dynamic number of personnel to be retrained and/or excessively complex, required procedures such as foreign exchange service calling procedures. The result is that communications system management, aware of the required network changes, resigns itself to the reality of a continued inefficient system with its associated lost value. It is therefore necessary that total calling usage visibility be provided in a timely manner by the CBX and that usage also be controlled by the same CBX system without significant personnel participation.

Alternative Network Services

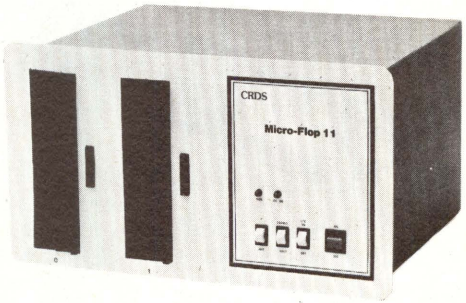
Since the CBX performs individual call routing decisions based on stored tables and instructions, user personnel have minimal call procedure participation. When personnel have no procedures to follow, it logically follows that they will have no procedures from which to deviate. This simplified fact constitutes the design philosophy of these CBX systems.

Many foreign exchange service applications that were not implemented due to calling procedure complexities are now totally feasible. A list of telephone company central office designations permitted to be reached via a foreign exchange service can be stored in the CBX memory. Whenever a call is entered for a telephone number in that remote central office, the connection is automatically established using the foreign exchange service without any participation or awareness of the call originator. This same automatic routing of outgoing calls to other communications facilities such as WATS also assures the proper placement of calls for minimum cost and maximum value.

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CIRCLE 10 ON INQUIRY CARD

Even local metropolitan and suburban areas in which the CBX is located can be called for greater value by the design and automatic loading of a local foreign exchange network. A typical metropolitan area could charge $0.25 for a 5-min call to the city's suburbs. Most intrastate tariffs provide businesses with a free calling zone if the call enters the public telephone network at a point in the suburbs. This zone can typically encompass an area of 10 to 15 miles surrounding the suburban telephone exchange. Foreign exchange services from the metropolitan-located CBX into various suburban areas can provide free local calling with automatic call routing based on the destination telephone central office designation. A monthly charge of approximately $100 is typical for a suburban foreign exchange service. Assuming it is only 50% utilized with these typical 5-min calls, a company would be paying only $0.104/call for a normal $0.25 call. Such a local network could reduce local calling cost by approximately 58%. Visibility of these local calls would permit the proper design of such a local network as well as allow its continued maintenance and management.

The lowest cost/call is only part of the calling value algorithm. The resulting network must, at the same time, provide the legitimate calling personnel with a grade of service that does not conflict with their calling availability. Few calls can actually be classified as emergency calls that cannot wait for a busy communications facility to become available. Most calls that bypass a busy WATS or foreign exchange facility incur toll charges because of the call originator's concept of convenience and efficiency. The call itself could wait a few minutes for an available facility, but the call originator does not want to continually attempt to find the desired communications facility's availability. In view of a better grade of service prompted by the call originator's requirements rather than the call's actual degree of urgency, most communications networks are configured with more trunks than are actually required.

Call queuing addresses the resolution of call urgency and caller's efficiency. When a CBX system, in attempting to automatically connect a call, encounters a busy facility, the call is placed into a waiting queue. This table in the CBX memory identifies the desired destination telephone number and location (extension) of the call originator. The table also must have the ability to prioritize these queued calls on a first-in, first-out basis similar in concept to that used in digital message or data switching system output message buffers. When the desired facility becomes available, the originator is then called by the CBX and the destination telephone number automatically dialed from the queue table. This capability has relieved the call originator of the time-consuming task of repeatedly attempting to access the busy communications facility or waiting for the facility's availability with the telephone in hand. The convenience and efficiency criteria of the typical call originator has been properly satisfied. Actual experience has shown a call queue duration of up to 10 min is easily absorbed by the calling personnel's peripheral business activities, resulting in virtually no call-delay complaints.

With respect to the communications network value, maximum loading on a minimum number of communications facilities can be realistically achieved and maintained. Analogous to the historical technique of switchboard operators' placing all calls for personnel, the resulting *experienced* grade of service is totally compatible with the vast majority of users.

This equilibrium between network cost and grade of service is particularly critical with the revised WATS tariff. No longer is usage and hence cost calculated on a per facility basis. The use of average line loading to determine cost renders the usual decision to add one more line considerably more significant than a few additional monthly dollars. If a present band 1 WATS trunk group has a total of five trunks and carries an accumulative usage of 23,500 min, the monthly cost would be $4643.50 with the revised tariff. This network configuration would typically present a call blocking factor of nine busy signals for every 100 call attempts (9:100-P09). By adding one more band 1 measured time WATS line, the grade of service would improve to approximately 3:100, yet the monthly cost would increase to $5030.06. This is an increase of 8.3%. Under the previous WATS tariff, that improvement in the grade of service would have increased the charge from $3900.50 to $3949.50, an increase of $49/month (1.3%).

It is therefore mandatory for every communications system manager to realize the network limitations imposed by these recent communications service tariffs. The increasing lack of provided visibility coupled with decreasing network design and configuration alternatives must be compensated for by computerized monitoring and control of these networks. It is equally imperative that the capabilities and functions that can be implemented in these computerized telephone systems be under the complete control of the communications network management and certainly not within the exclusive domain of the vendor of the associated communications facilities and services. It is encouraging to note that through these network management techniques provided by computerized control, communications network value can be not only maintained but also improved, in spite of the continuing philosophy of the communications tariffs to deny such visibility and control to responsible communications network management.

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CIRCLE 13 ON INQUIRY CARD

Programmable Controller Approved for SDLC/HDLC

Data communications network protocols require considerable interface intelligence because of the high level decisions and responses being transmitted and received. To fill this need economically, a programmable multiprotocol MOS LSI device, developed by Standard Microsystems Corp, Hauppauge, NY, processes both SDLC and HDLC protocols.

COM 5025 is a 40-pin monolithic IC that uses the COPLAMOS® n-channel silicon gate process and operates at speeds to 2M baud. The universal synchronous receiver/transmitter provides dedicated control and implementation of major protocols, including bit-oriented types such as SDLC, HDLC, and ADCCP, and byte-oriented BISYNC and DDCMP, and is the first programmable chip controller approved for these protocols. It is processor-compatible (8- or 16-bit), and direct TTL-compatible, and contains selectable protocols and a 3-state input/output bus. Data, status, and control registers are double buffered. Full- or half-duplex operation is provided by means of independent transmitter and receiver clocks.

Data lengths are individually selectable for receiver and transmitter from one to eight bits. Data, status, and control registers are linked to a master reset which initializes them to SDLC protocol on power-up. A built-in maintenance feature tests operation of the chip by performing data loop-around internally.

The controller is responsible for all higher level decisions and for interpretation of some fields within message frames. The degree to which this occurs is dependent on the protocol being implemented. Receiver and transmitter logic operate as two totally independent sections with a minimum of common logic.

For bit-oriented protocols such as SDLC, HDLC, and ADCCP, the device provides bit stuffing and stripping, automatic frame character detection and generation, and residue handling. Messages which terminate with a partial data byte are accompanied by the number of valid data bits available.

Options for bit protocols include variable length data (1- to 8-bit bytes), error checking—16-bit polynomial CRC (or CCITT)—primary or secondary station address mode, extendable address field to any number of bytes, extendable control field to two bytes, and idle mode to transmit flag characters or mark the line.

For byte-oriented protocols, automatic detection and generation of SYNC characters is provided; options include variable length data, variable SYNC characters (5, 6, 7, or 8 bits), error checking—16-bit polynomial CRC (or CCITT)—as well as odd/even parity, deletion of leading SYNC characters after synchronization, and an idle mode to transmit SYNC characters or to mark the line.

The chip is compatible with specifications described in IBM General Information Bulletins GA27-3093 and GA27-3098 and *IBM Systems Journal*, Vol 15, No 1, 1976 (G321-0044), EIA Standard RS-334, CCITT Standard X.25, and ANSI X353 and XS34/589. Typical cost (in 500 to 999 quantity) is $61.40/unit.

Circle 400 on Inquiry Card

Tests Study Use of Fiber Optics in Secure Communications Systems

Three advanced development models of fiber optics, built by International Telephone and Telegraph Corp, Hughes Aircraft Co, and Harris Corp, are being studied by the Electronic Systems Div of the Air Force Systems Command as a way to protect communication of sensitive information. Tests are being conducted by the Sandia Laboratory in Albuquerque, NM, and the Optical Communications and Components Laboratory of Rome Air Development Center's Deputy for Electronic Technology at Hanscom Air Force Base, MA 01731.

Optical fiber communications, which have no radiation of signals to give away message content, are being extensively tested to determine if they can resist attempts to tap into communication circuits, the degree of protection they offer, and their full capabilities. Fiber optics is expected to offer greater message handling, lighter equipment, and lower overall system cost. Next phase of the development program will be based on results of this evaluation.

Switching Systems Achieve More Throughput With Processor

Designed for high efficiency control of telegraph, telex, and teleprocessing networks, the DS 714/81 version has been added to the DS 714 computer-directed message/data/circuit switching systems. It is based on an advanced CPU (also compatible with the other family members) which provides more flexibility and traffic handling capability.

Data I/O functions are divided optimally between software and hardware operating under control of specialized microprograms. Available operational modes include message switching (store-and-forward), core-cut-through (direct retransmission), push (analogous-to-true circuit switching), monitor (combination of core-cut-through and message switching), and high speed data chaining.

The core memory used in the processor has an access time of 300 ns and a complete cycle time of 700 ns. Schottky-TTL technology is used in the circuitry with high speed requirements; semiconductor RAMS are used to accommodate the 64 index registers. Execution time has been reduced from 6 to 2.4 μs, and time to input and retransmit a data character in the message switching mode has gone from 22 to 4.6 μs.

Existing software can be used with the processor. In addition, DACOS (Data Communication Operating System) has been developed by Philips Telecommunications, PO Box 32, Hilversum 1301, The Netherlands as a modular real-time system with multiprogramming on up to 16 levels and multitasking facilities.

Various multiprocessor configurations are possible. Further enhancements are a family of intelligent multiplexers designed to handle specific or mixed types of traffic.

Circle 401 on Inquiry Card

Smart Communications Terminals Handle Multiple Applications

A line of communications terminals with the intelligence to handle multiple applications concurrently is aimed at moving the communications field toward "consolidated networking," rather than having multiple systems each with its own network and terminals. The standalone Smarts terminal controller has three microprocessors and floppy disc storage providing general-purpose communications terminals with a powerful operating system for file management, communication control, and editing. The controller is manufactured by Scientific Micro Systems, Mountain View, Calif to the specifications of Western Union Data Services Co, 70 McKee Dr, Mahwah, NJ 07430. Shugart Associates supplies the disc.

(*Continued on p 20*)

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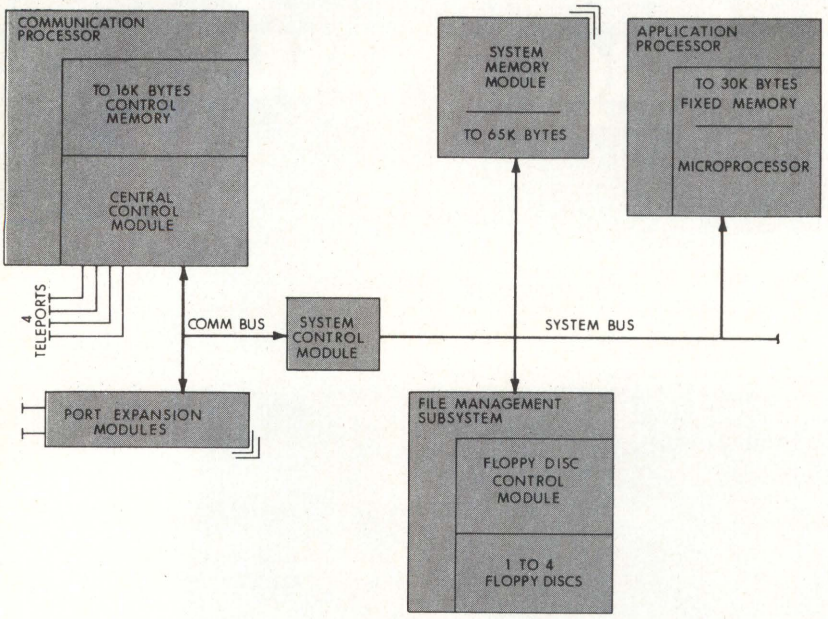
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CIRCLE 14 ON INQUIRY CARD



Architecture of Western Union Data Service's Smarts Controller. It contains three functionally-oriented microprocessors for fast response and efficient throughput. Basic system has communications, file management, application, and system memory and control module boards. The last creates data bus and determines which module can access system bus or data path, based on established priority

The communications processor is an SMS 300 which acts as the communication front end, executing instructions in 300 ns. It handles all line servicing, modem control, and protocol, and integrates all terminal devices.

Operating at 300 ns, the disc controller (an SMS 300) dynamically allocates and deallocates disc space, maintains all required directories, and randomly accesses files. A single disc storage unit stores 270,000 characters in up to 60 operator-named files.

A Zilog 80 serves as the applications processor, performing all editing, providing basic terminal control, and acting as the command interpreter.

The controller supports concurrent operations in batch or conversational mode. The terminal can be polled at any time without interrupting the operator.

Formats can be created by the operator, or downloaded from the host computer. They are accessed by format name, and can be stored in a supervisory file for protection. It is a prompted format system, rather than full text format.

Self-testing of the controller's operational functions is automatically initiated when power is turned on or when power interruptions last more than 8 ms. The operator is informed when the terminal is ready for operation, or when a problem exists.

Offered in a variety of terminal configurations, the controller will initially be configured with a command console and local printer. Deliveries will begin in the third quarter of 1977. The controller is equipped with four ports—two communication ports that operate at 1200 baud, and the other two for the console and printer. By first quarter of 1978, models operating at 2400 and 4800 baud will be offered.

Prices start at $235/month on a 3-year basis. This includes a keyboard printer, 1200-baud modem, and maintenance provided by the Centralized Termicare System and nationwide service centers.

Circle 402 on Inquiry Card

Remote Job Processor Operates Concurrently With Other DXS Functions

Allowing simultaneous online interaction and batch transmission with a host computer, the Remote Job Processor (RJP) 2780/3780 emulation package runs concurrently with all other functions on the DXS Data Exchange System. It supports multiple RJP lines to allow data transfer to one or more hosts or RJP terminals. Emulation is controlled by a set of menu-driven inquiry/response screens from model 914A video display terminals. Functions provide for easy management of control parameters, job creation and submission, statistics, and emulator status display.

In addition, the package from Texas Instruments Inc, Digital Systems Div, PO Box 1444, M/S 784, Houston, TX 77001 allows transfer of disc and tape files, including DXS Terminal Source Editor library members. Use of disc files and spooling of I/O compensate for the absence of multileaving. Set of data stream control records permits execution of additional functions.

Communication will operate in half-duplex mode; 4-wire (duplex) lines can be used by some data sets to minimize line-turnaround time. Dial-up line support includes auto-answer if that option is provided on the modem. Package is priced at $2750.

Circle 403 on Inquiry Card

Cost/Utility Benefits of Message Switching System Aid Public/In-House User

As a continuing advance in the utility of message switching for business communications, Tymnet, Inc, 10261 Bubb Rd, Cupertino, CA 95014 has announced the OnTyme System, available both as an FCC authorized public message switching service and as an in-house facility. Designed for organizations of all sizes, the system provides fast, accurate written communications between geographically dispersed locations at a cost-effective rate.

The system has evolved from three technologies: store and forward message switching, online computer systems, and packet data communications. Users have a choice of terminal equipment, as most 110- to 1200-baud terminals can be used in any combination. These terminals are not dedicated solely to message com-

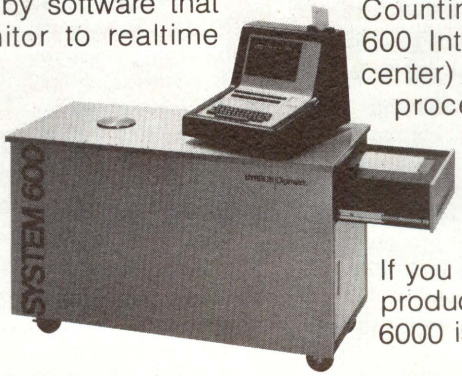
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Begin with the 6015 processor drawer containing a 6800 processor with power supply, 32K bytes of static RAM, room for 8 I/O devices, and our total software package. Add RAM via 16K, 8K or 2K boards up to 64K, and select I/O boards to fill your needs: everything from an ICOM floppy controller to a dual slope A/D, or a control card with 8 independent triacs. Of course there are standard peripheral cards such as a dual 9600 baud EIA RS232 port, and an 8-bit duplex 80 kilobaud TTL interface. We also have a 10 digit BCD input card and a general purpose I/O board if you must design your own. Those little things, such as a realtime clock and priority interrupt hardware are standard.

Digimetric may be young in marketing mainframes and boards, but we have been building microprocessors into products for quite a while so we know your needs and problems. The 400 Series Counting Scales, and our System 600 Intelligent Work Station (shown at center) are good examples of our microprocessor experience. From single board applications to full systems, we have designed our products for tough, cost competitive environments.



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CIRCLE 15 ON INQUIRY CARD

munications; they may also be used for applications such as interactive timesharing or data base inquiry.

As the principal communications resource, the TYMNET public packet network brings packet technology to message switching users. Complementing TYMNET is WATS which allows access to and from user terminals throughout the country.

Service users have the capability of an advanced store-and-forward system without the capital expense and management of a private system. The system can be installed in-house at any time without changing terminals or operating procedures, and without losing benefits of TYMNET. It is modified to meet individual needs, and can be interfaced to the customer's other computers. With in-house use, public service can be used as backup and to send messages to terminals on the public network. In-house users also can concurrently execute user-written programs.

Features include online inquiry of message status security procedure to control authorized use, message control numbering, group coding of destinations, online retrieval of recent messages, and provision of traffic analysis data for management control. Most data terminals can be connected with the user-oriented interface.

Fees for the public message switching service include a $100/month service charge/customer, $0.05/message sent, and charges for terminal connect time and characters transmitted. Optional data storage is also available. Average cost of a typical message (500 to 1000 char) is in the $0.30 to $0.40 range. Costs of the in-house version range from $120,000 for small, single processor systems to approximately $300,000 for large, redundant systems with extensive tailoring.

Microcomputer-Based Processor Systems Lead to Third Generation Networks

As the result of a 3-year development program, Telenet Communications Corp, 1050 17th St, NW, Washington, DC 20036 has announced a family of intelligent communications processors which will permit customer computers and terminals to plug into the company's public packet network without hardware or software changes. They will be available to customers beginning in the third quarter of 1977.

Beginning this year, the microcomputer-based systems also will be incorporated into the network as packet switches and data concentrators, forming a "third generation" architecture for packet networks. Improvements in cost performance, services, and reliability should be realized.

The TP-1000 processor is designed as a network access device for customer host computers which need to support only a few remote asynchronous terminals simultaneously on the network. It can also function as a concentrator to link small clusters of terminals at remote customer locations to the network.

The second version, TP-2000, serves as a larger-scale network access device for hosts which support from 12 to 32 remote asynchronous terminals simultaneously. It can be configured with redundant microcomputers for each internal subsystem and utilizes the international standard X.25 packet-mode network interface protocol.

Circle 404 on Inquiry Card

2-Way Communications Between Systems Offer Cost-Effective Solutions

Effective 2-way asynchronous or bisynchronous communications between any IBM System/3 (S/3) equipped for telecommunications and the System 99 small business computer provide cost-effective methods of solving distributed data processing needs for small businesses. Using a 1200-baud model 9666 IBM channel adapter, model 9665 asynchronous modem, and/or model 9650 communications package, all from GRI Computer Corp, 870 Georges Rd, North Brunswick, NJ 08902, the System 99 can intercommunicate with any S/3 having 1200- to 4800-baud bisynchronous communications facilities. Standard IBM protocol is binary synchronous communications (BSC).

For S/3 users who need remote processing facilities or real-time capabilities, the System 99 provides additional telecommunications capabilities. The added features also allow the System 99 to serve as a compatible replacement or upgrade for any IBM BSC terminals in distributed data processing networks using most IBM computers.

Features permit online data collection, and offline or online batched data transmission. Online conversational transmissions are possible between System 99 and its own terminals through the Interactive RPG II. Transmission is in half-duplex mode over switched, leased, or private lines; either ASCII or EBCDIC codes may be transmitted.

The 9666 channel adapter, priced at $600, must be purchased with the 9665 modem, costing $645. It is used with the 9650 communications package which sells for $4335.

Circle 409 on Inquiry Card

OS Console Support For Virtual Data Link System Increases Throughput

Providing a level of control for remote site users similar to that available from an installed processor, the console support package allows users of distributed networks to replace IBM HASP or JES multileaving workstations with PIX II virtual data links. The data links operate at throughput rates up to twice that of IBM workstations.

The package is offered by Paradyne Corp, 8550 Ulmerton Rd, Largo, FL 33541 to permit users at remote sites to control jobs transmitted to central mainframes under synchronous data link control (SDLC) protocol. VTAM/NCP teleprocessing software normally implemented to support SDLC protocol is not required; also eliminated is the RTAM software normally needed to support multileaving workstations.

The package allows systems to operate as HASP workstations under OS/MFT, /MVT, or /vs2-SVS; and as JES workstations under OS/vs1 or /vs2-MVS. Full tape drive support and SDLC communications are provided under any of those operating systems.

At each remote site, control is provided for up to 24 peripheral devices, including card readers, printers, tape drives, and interactive terminals operating concurrently as if they were locally connected to a mainframe. Consoles attached to a remote control unit in a configuration function as if they were IBM 3277, 3215, or 1052 devices. The system also allows users to receive OS messages associated with their jobs.

The data link, rather than the software of the host processor, performs both data compression and multileaving functions. Software to support the console package is available to system users at no charge; the console adds approximately $125/month to the system's cost.

Circle 405 on Inquiry Card

Direct input and output of analog and digital signals to your computer.

RTP is a family of standard products that allows direct input and output of analog and digital signals to your general purpose digital computer.

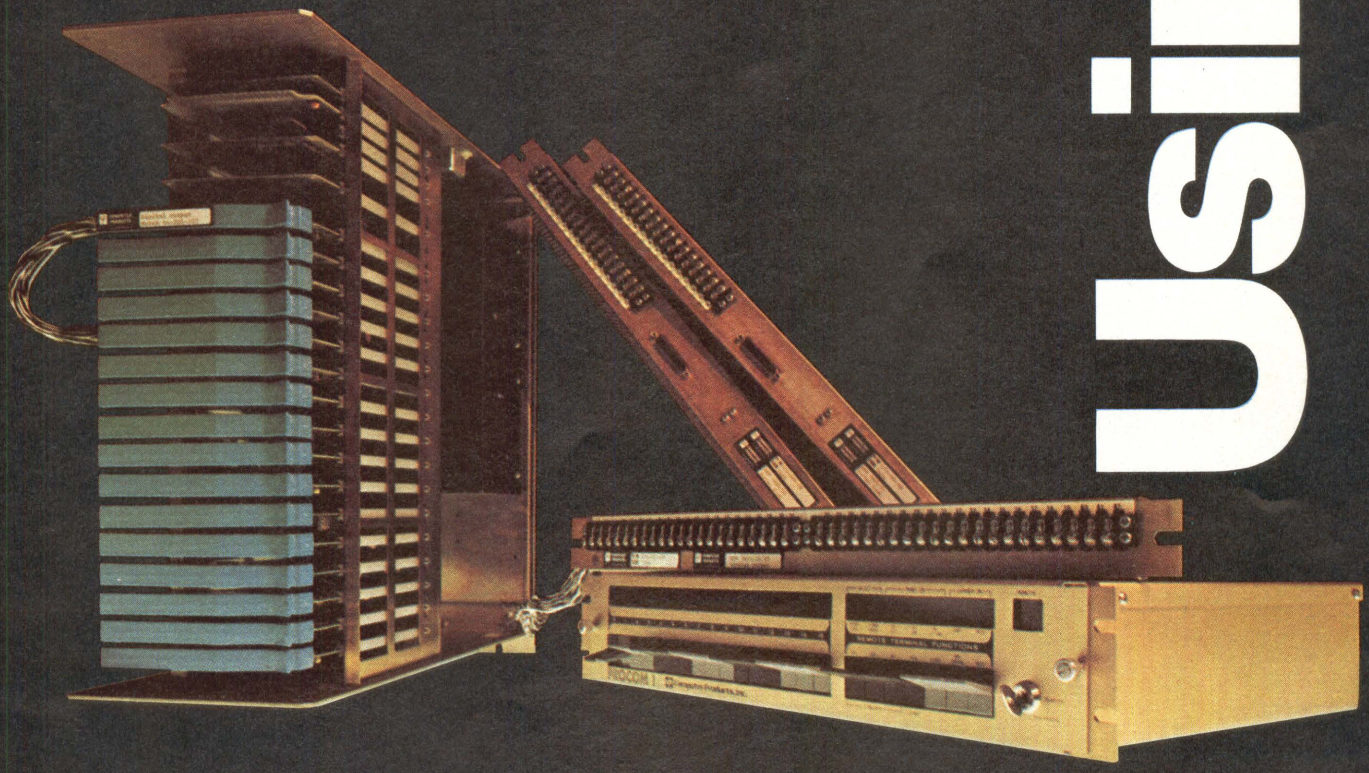
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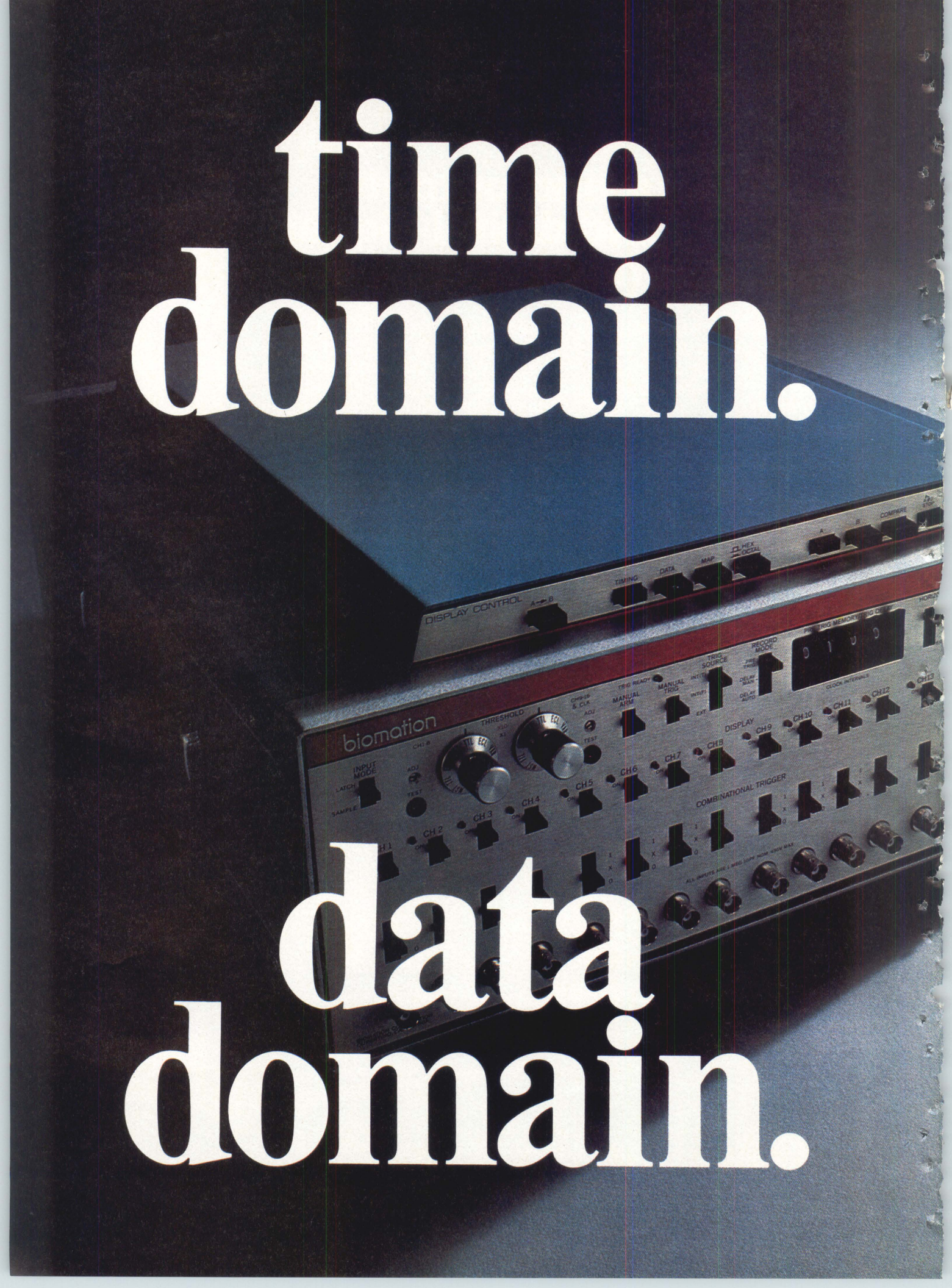
Using RTP.

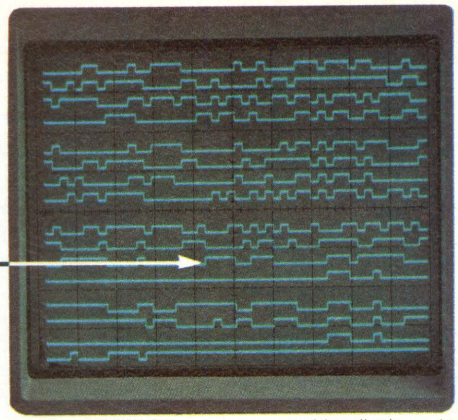


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CIRCLE 16 ON INQUIRY CARD


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MANUAL ARM
MANUAL TRIG
TRIG SOURCE
RECORD MODE
DISPLAY
COMBINATIONAL TRIGGER
INPUT MODE
SAMPLE
LATCH
TEST
CH 1
CH 2
CH 3
CH 4
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CH 6
CH 7
CH 8
CH 9
CH 10
CH 11
CH 12
CH 13



Biomation's new 1650-D produces a repetitive display output reconstructing precisely 500 bits per line for a 16-line timing diagram on a conventional oscilloscope or CRT display. Separate selection of individual channel outputs allows viewing of 1, 2...16 channels at one time with automatic vertical expansion.

Biomation's new logic analyzers give you both.



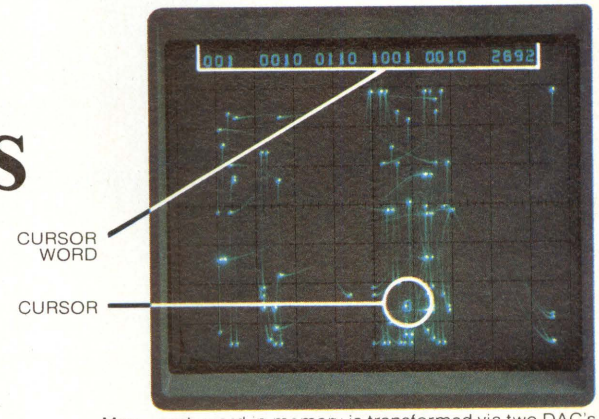
When your job is to interface, integrate and program a complex new digital logic system, you want as much information as you can get.

That's why we're providing a new set of tools which let you display timing information as well as logic word content—in the language of your choice.

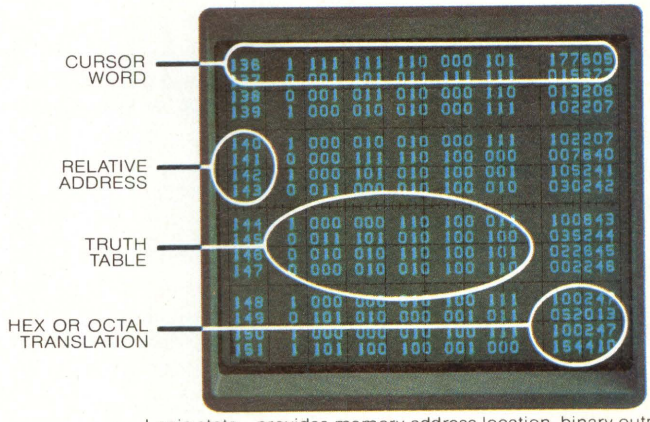
Our new 1650-D logic analyzer gives you 16 channels at 50MHz. Our 851-D gives you 8 channels at the same speed. Accessories can now give you a logic state (1's and 0's) display of any 16 stored words; hex or octal translation; and a vector map of memory contents. The 8 and 16-channel logic analyzers feature:

- Pretrigger and delayed trigger recording
- Trigger point can be easily identified
- Latch record mode for fast pulse capture
- Combinational triggering (true *or* false)
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- Display expansion, mixed or full, X5, X10 or X20

These are complex instruments and we can't give you all significant details here. But please write, call, or use the reader service card. We want to get this useful information into your hands. Biomation, 10411 Bubb Road, Cupertino, CA 95014, (408) 255-9500. TWX: 910-338-0226.



Map—each word in memory is transformed via two DAC's to form a unique dot which characterizes that word. All 512 words of the 1650's memory can be accessed for mapping. The cursor word is circled in the map as well as displayed at the top of the screen in alphanumeric form. The cursor may be moved to any of the points in the map for positive identification of that word. In addition, a map of only 16 words may be selected.



Logic state—provides memory address location, binary output of the 16 channels and selectable octal or hexidecimal translation. 16 words are displayed at one time with the cursor address location at the top of the screen. Movement of the cursor control allows accessing any 16 words of the entire 512 words stored in the 1650-D. The display control memory can store 16 words while a different set of 16 is selected from the 1650's main memory (or a new recording is made). These two sets of 16 words can then be overlayed on the CRT. *Any differences will blink* and be easily identified.

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CIRCLE 17 ON INQUIRY CARD

Use of Fiber Optics Is Predicted by Mid-Eighties

Cost-effective broadband communications capabilities beyond those of hardwire systems may be available by the mid-1980s through fiber optics. However, more research, development, and testing of single-fiber technology is needed to achieve optimum design of cable and associated components from both cost and performance viewpoints; it will be cost-effectiveness which will determine the success or failure.

R. Warren Howe, vice president-marketing of Belden Corp, Geneva, IL 60134, foresees "fiber optic cables selling in significant volume, but at levels that penetrate less than 10% of the total wire and cable market as we know it today." He also added that the lightguides will not be required for several years as a standard item in an electronic distributor's product inventory.

Belden Corp designed and jacketed a prototype cable of six optical fibers used in July 1976 by Teleprompter Corp in the first domestic transmission of cable television signals by lightwave techniques. Achievements in cable design and manufacturing technology, as well as in development of connectors and associated system hardware, have been successful. Other end-user evaluations are continuing of low signal-loss characteristics of the single-fiber lightguides for traditional electronic industry markets; today, fiber optics is in a market-testing phase.



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Tariff Revisions of Private Line Services Are Announced

A revised tariff structure for private line services of the Southern Pacific Communications Co, Burlingame, CA 94010 is aimed at achieving rate stability. Subject to FCC approval, the company intends to offer these services for either a 6- or 24-month commitment, as well as the present 30-day agreement, to meet both telecommunications needs and requirements of specialized common carriers.

Long-term services will be billed at rates below present short-term commitment prices. Prior to 15 days before the end of the service period, a customer can discontinue service; otherwise, terms will automatically be renewed at the prevailing price. A fixed price will be maintained throughout the 6-month period.

On a 2-yr agreement, the first year's rate will be firm, after which prevailing rates will be charged as long as increases are not more than 10% of the original service.

Anticipated Impact of Revised WATS Portends Numerous Changes

Massive restructuring in Wide Area Telephone Service (WATS) tariffs, coupled with the elimination of Tel-

pak and a rise in Dataphone rates, will have a "profound" impact on most larger businesses, with users facing an impending upheaval in services and costs. The tariffs call for elimination of fixed-cost pricing, establishment of a tapered usage-sensitive rate structure, regrouping of In- and Out-WATS geographical areas, and a shift in relative pricing levels of those services.

This assessment by Harvey L. Poppel, senior vice president of Booz•Allen & Hamilton, 245 Park Ave, New York, NY 10017 is based on a computer-assisted analysis of the rates. Several conclusions have been drawn. Heavy users face substantial cost increases; users of longer distance WATS may want to investigate leased-line alternatives. Smaller businesses may now find some services within their reach.

It will be more difficult to piggyback specialized usages other than voice communications (eg, data and facsimile) on WATS; alternatives, such as specialized data services, will be sought. Other significant migrations to and from WATS will occur. Long distance calls may be switched from WATS to toll; nighttime use of WATS may be less cost-effective; and inbound WATS costs may now be affordable.

Computer-controlled or computer-monitored WATS users will face unanticipated reprogramming costs. Smaller users unable to afford computerized controls will have to consider funneling access to previously dial-accessible WATS through phone operators.

The restructuring will force users to change their mix of WATS lines. The rates will require intelligent design and tight management control.

Terminal Monitor System Supports Operation of Interactive Applications

Common application program interface between the operating system (os/vs) and user-written programs is provided by a terminal monitor system, along with an online data management capability which enables data compression without space reorganization. In combination, the system's software can maintain line-image, structure data transactions, and support source program library, interactive processor, process control device, and application management.

The system operates in a dedicated or multiprogramming environment, with services accessed by a 360/370 Supervisor Call routine. User-written programs may be in ANS COBOL, PL/1, FORTRAN, or assembly language.

Features include terminal-to-terminal message switching, control over editing and printout, and provision for remote batch job entry. Security is provided by project identifier codes and passwords. Aspen Systems Corp, Germantown, MD 20767 has designed the system to operate on IBM 360/40, 370/135, or larger computers, supporting most typewriters and display and printer terminals.

Circle 406 on Inquiry Card

Processing Systems With Workstations Meet Batch-Terminal Needs

Two IBM-compatible, batch-terminal devices for the 3650 and 3670 communications processing systems, announced by Comten, Inc, 1950 W County Rd B-2, St Paul, MN 55113, are the 7780 and 7781 HASP workstations. Both use the system's communications resources for workstation control, eliminating the need for separate control hardware.

The 7780 minimum configuration consists of a 600-card/min reader and 600-line/min printer, with an option to share the system console for operator communications. In addition, the 7781 has its own dedicated console.

Both can be expanded to include up to six additional card readers and six additional line printers. Peripherals included in the workstations are the company's 7305 card reader, 7406 line printer, and 4008 console.

Workstation control is provided by adding two programs—multileaving adapter module and multileaving workstation emulator—to existing network-control software in the processing system. Additional features include multiple workstation support from a single processing system, dynamic reassignment of peripherals among workstations, and enhanced terminal restart capabilities.

Shipments are scheduled for mid-September, with initial deliveries to remote nodes in the company's communications networks supporting IBM

8-BIG DISK, 4-CPU μCONTROLLER for DEC/DGC software

The new AED 8000 mass storage system with microprogrammable controller can be completely integrated into your DEC or Data General system. You can now enjoy patch-free use of any OS changes generated by the mainframe manufacturer, because AED's emulation capability ensures continuous compatibility to standard software. Add to this AED 8000's unique ability to serve up to 4 CPUs per controller at the same time, its built-in Error Correction System, and a multiple-register scroll that displays mainframe register information plus valuable diagnostic data, and you'll see why the AED 8000 is way ahead of the competition. AED's field-proven reliability and fast 45-60 day delivery make the AED 8000 mass storage system a serious contender for your disk dollars.



Compare these features

	AED 8000	DEC DGC
Megabytes per drive	67.4→250	40 92
No. of drives per controller	1→8	8 4
Megabytes per controller	540→2,000	320 368
No. of CPU's per controller	4	1 2
16-bit transfer rate	1.6 μs	6.4 μs 2.5 μs
16-bit buffer	256	6 8
Error Correction Code	by controller	none
Bootstrap	IPL in controller	CPU ROM
Micro-processor	40 ns. 24 bits	none
• Emulates DEC/DGC controller	yes	—
• Macro Instruction Code	yes	none
• Data Scanning & Management	in controller	in CPU
• Variable Sector Length	yes	none
• CPU to CPU transfers	bypass the disk	none via disk

Price: Quantity 1 $20,250 incl. 67.4 Mbyte drive

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CIRCLE 19 ON INQUIRY CARD →

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With the success of their Athena 2000 home sewing machine, today we may look even better.

This revolutionary new machine by Singer can sew 25 different stitch patterns at the touch of a button. And it's entirely controlled by a single MOS circuit made by AMI.

Singer eliminated 350 mechanical parts by redesigning around this dense little chip. At the same time, they added immensely to the performance and safety features of the machine.

We did such a good job on the Athena machine that Singer gave us the contract for their next two models of electronic sewing machines.

Singer chose AMI because of our reputation for solving MOS problems quickly, confidentially and economically. In the past eleven years, some of the world's biggest companies have come to us for the same reasons.

We're designing custom chips for many Fortune 500 companies like Singer. With your reputation riding on every product that you make, maybe you'd better take a good look at us, too. Write to Custom Product Marketing, AMI, 3800 Homestead Road, Santa Clara, California 95051. Or contact your local AMI sales office. It could be the beginning of another success story.

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CIRCLE 20 ON INQUIRY CARD

System 360 or 370 host computers. Additional deliveries to systems at host sites are planned for the first quarter of next year.
Circle 407 on Inquiry Card

Digital Technology Is Future Basis of Communications Field

Computer and voice communications technologies are becoming more and more alike. That was a key point made by Robert C. Scrivener, chairman of the board and chief executive officer of Northern Telecom Ltd, when he addressed the Thirtieth Annual Meeting of the International Communications Assoc in Toronto, Ontario, Canada on May 16. He voiced his satisfaction "that the future is digital. . . . Had we had the digital technology 50 years ago, we would have gone from manual to digital and wouldn't have started on analog at all."

He pointed out that "digital maximizes the potential of the basic thrust of integrated circuit and software technology as it has developed and will be developing. To telephone companies a digital switch won't cost any more than the equivalent analog switch, but an all digital network will reduce operating and capital costs by at least as much as 20 percent as compared to analog."

As Mr Scrivener noted, telephone companies are in preferred positions. They don't yet have huge investments, and tax laws encourage them to modernize quickly. The "companies can't wait, but must have voice-data compatible networks now, in order to compete and cut costs. The digital savings will depend on each situation, but digital flexibility opens all future options." Although it will require a long time to replace analog investments, fully digital equipment is already appearing—such as telephones, terminals, processors, transmissions, and switches that combine to make up complete communications.

However, as computer and voice communications come closer together it becomes necessary to maximize the effectiveness and productivity of skilled, knowledgeable workers. The technology, once available, must be worked into layouts that are esthetically pleasing, economical, and flexible, all while being tied into the massive memory, speed, and capacity of the digital world. It will be the skills of the designers together with the potential of both IC and software technologies that will form the communication markets of tomorrow.

With the interconnect debate, Scrivener personally feels that it will be competition rather than government regulation that will produce better results. There is absolutely no merit, though, in risking the destruction of the world's best and lowest cost telecommunications that exist in the U.S. and Canada due to disputes between industry and government.

To date, the best results have been obtained by the integrated approach to telecommunications service evolved by Bell System in which operations, research, and manufacturing are linked under common ownership. It has been emulated in Canada and by other countries around the world.

Changes and developments in the telephone business in North America are being led by events in the U.S. At the same time, the close connection of Canada with the Bell System has resulted in the Canadian telecommunications network, its service, and technical standards, which for all intents and purposes are the same as those of the U.S.

The common standards and service philosophies between the two countries has, in many respects, formed a homogenous market for suppliers. For instance the products designed for initial introduction in Canada by Northern Telecom, Inc (the U.S. subsidiary) are now also produced in the U.S.

Optimum Price/ Performance Features of Products Enhance CBX

Contained in "Release IV Software," a package of products for the Computerized Branch Exchange (CBX), are seven major optional, 16 standard, and several enhanced features. The major functions announced by Rolm Corp, 4900 Old Ironsides Dr, Santa Clara, CA 95050 are Automatic Call Distribution (ACD), Centralized Attendant Service (CAS), Satellite Operation, Expanded Traffic Capability, Inward Call Detail Recording (ICDR), Message Registration, and Standby Queuing. Among the standard features available are Trunk Time-of-Day Access, 1000 Number System Speed Calling, and Off-Hook Routing.

For organizations with high incoming telephone traffic from customers, the ACD provides automatic, load-shared distribution of incoming calls to a team(s) of available "agents." When all agents in a team are engaged, the CBX connects callers to a delay announcement, then places music on the line. Delayed calls are answered as agents become available according to priority and order of receipt. A second delayed call announcement to a holding caller or overflow group can also be provided.

The ACD supervisor may perform agent call monitoring, remotely control status and forwarding of agent positions and groups, and dynamically reconfigure ACD operation to meet varying traffic loads and special situations. Traffic statistics are continually gathered and displayed on an optional CRT or printer. Four display types are current status, cumulative statistics, trunk group statistics, and agent performance/status information.

The CAS serves organizations having multiple installations, by allowing all attendants to be grouped at one location, where all incoming calls are handled. Significant manpower reductions, better telecommunications system management greater attendant security, and closer attendant supervision may be achieved. Features of standard CBX operation are unchanged by the addition of CAS; normal CBX attendant service can also be provided at any of the CAS locations.

Satellite Operation provides a method of conveniently handling applications involving multiple geographically separated installations in one area. Centralized trunking, attendants, and call detail recording are provided by this option.

The Expanded Traffic feature allows the CBX user to obtain detailed data on the traffic carried by the CBX so that trunk facilities can be configured for optimum user economics. Inward Call Detail Recording allows the user to obtain data on which stations are receiving calls from which trunks, and the duration of these calls. This is particularly useful for users having In-WATS who wish to allocate costs to various departments within the organization.

Release IV features will be incorporated into CBX systems scheduled for shipment after Sept 30. They will be available for reconfiguration of previously installed CBX systems after Nov 4. □
Circle 408 on Inquiry Card





Data General. A la carte.

Now, you can buy our DASHER™ terminals, even if you don't own a Data General computer system. Select our fast impact printer and our user-oriented video display. Both are interface-compatible with any standard computer system.

Choose either 60 or 30 cps versions of the DASHER printer, which has a standard typewriter keyboard, u/l case, 132 columns.

DASHER display features a 1920 character screen, u/l case, convenient detached keyboard, programmable function keys, and a monitor that tilts and swivels.

Just as DASHER terminals' features make them easy to use, their attractive appearance makes them easy to fit into any environment. And of course they are solidly reliable and easy to maintain, a Data General trademark. For more details call your Data General sales office or nearest independent supplier of Data General terminals. Or send the coupon. Even a bit of Data General in your computer system is better than none.

Send details on ☐ DASHER printers ☐ DASHER displays
☐ Have salesman call.

I'm interested in _____ / _____ terminals.
no. type

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Title _____

Company _____

Address _____ Tel. _____

City _____ State _____ Zip _____

Mail to: Data General, Westboro, MA 01581

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CD-8

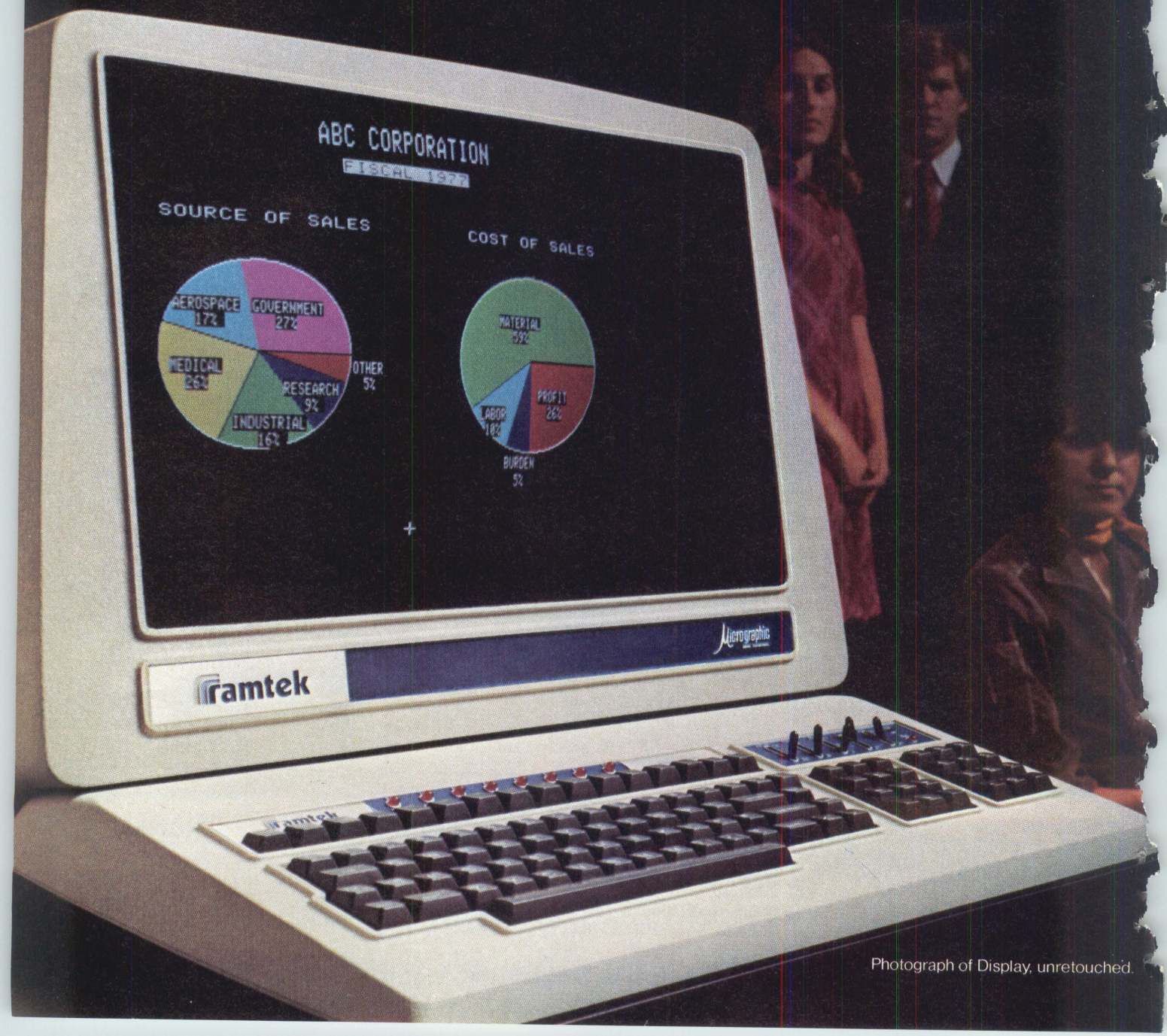
Data General

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Data General, Westboro, MA 01581, (617) 366-8911. Data General (Canada) Ltd., Ontario. Data General Europe, 15 Rue Le Sueur, Paris 75116, France. Data General Australia, Melbourne (03) 82-1361.

CIRCLE 21 ON INQUIRY CARD

Look what Ramtek has done to graphic terminals.



Photograph of Display, unretouched.

Now you can get quality resolution and a combination of true graphics and true alphanumerics at an affordable price.

Ramtek introduces the new Micrographic Terminal. No longer do you have to settle for poor resolution or give up color in economy priced display terminals. Ramtek gives you a high resolution, flicker-free display on a resolvable matrix of 512 elements by 256 lines. And you get a choice of black and white or any 8 of 64 colors as well as split or dual screen capability. The independent alphanumeric refresh offers you single character addressibility within a visible matrix of 25 rows of 80 characters that are crisp, sharp and well defined.



Ramtek's Micrographic Terminal is controlled by a powerful Zilog Z-80 with 28K bytes of PROM and 16K bytes of RAM.

In addition you can program the Ramtek Micrographic Terminal and give it the dedicated capability and intelligence you need for your application. Ramtek's software gives you TTY compatibility and high level graphic functions commanded by ASCII text strings. You can choose from an extensive list of options such as floppy disc interface, additional serial I/O ports, alphanumeric overlays, user defined fonts, color selections and packaged software.

More good news: prices for a black and white basic system begin at just $4,700 and for color at only $5,400.

But to fully appreciate the contribution the Ramtek Micrographic Terminal can make to your application, you'll need to know more details. Just call or write Ramtek Corporation, 585 N. Mary Ave., Sunnyvale CA 94806. If you're really in a hurry call us at (408) 735-8400 and ask for Todd Martin.

ramtek

Our Experience Shows

CIRCLE 22 ON INQUIRY CARD

Printers Fill Price/Performance Needs In Expanding Peripheral Market

Geared to meet all computer output printing needs—speed, quality, cost, and reliability—and reflecting many technical innovations, recently introduced printers illustrate the importance currently placed on peripherals by manufacturers. Among the technologies being used are thermal and impact matrix, ink jet, needle, and laser beam techniques. Performance covers the incredible range from 80 char/s to 21,000 lines/min (1 to 350 lines/s).

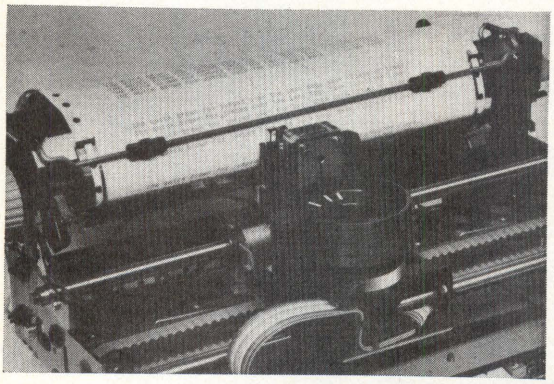
Medium, Low Speed Units

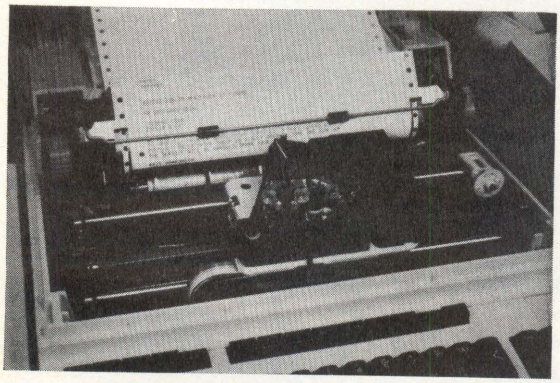
To reach the rapidly growing market found in the small business and terminal application areas, Dataproducts Corp, 6219 DeSoto Ave, Woodland Hills, CA 91364, developed its T-80 thermal matrix printer, which uses a nonimpact, single thermal dot matrix printing head to offer speed of 80 char/s. Priced at under $1000 (OEM quantities), the unit has nearly three times the speed of other units selling in that range.

High quality print at those speeds is attained by use of a proprietary thermal print head. This device, rather than applying constant heat to the matrix wires and lifting and moving the head from the paper to form each character, leaves the printhead in constant contact with the sensitized paper. Matrix wires are alternately heated and cooled as the head moves left to right across the paper. This pulsed heating effect permits high print speeds and simplifies printhead mechanics.

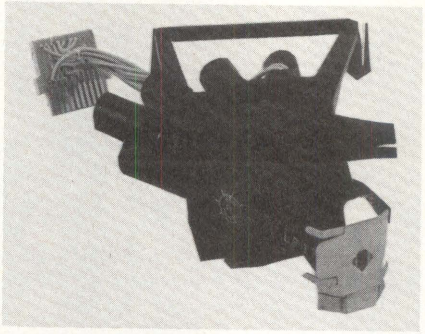
Circle 140 on Inquiry Card

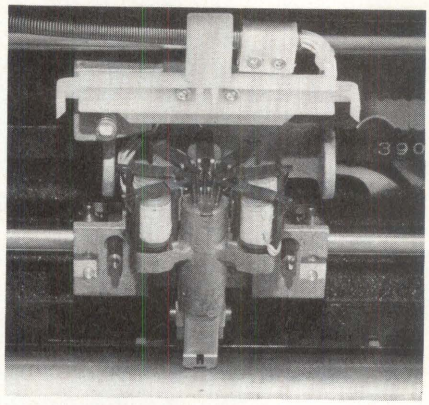
Operating in approximately the same speed range as the thermal printer, the PT-80 printer terminal from Siemens Corp, 186 Wood Ave S, Iselin, NJ 08830, is a highly modular unit that offers a choice of needle or ink-jet printing and paper tape or magnetic tape cassette for storage. Keyboard, printing mechanism, power electronics, interface adapter, power supply, control panel, and central device controller are housed in a desktop unit. All modules are connected to the single central control board via plug-ended cables and may be replaced quickly without adjustments or alignments.





Modularity of the PT-80 printer terminal allows users to select needle or ink jet printing, depending on speed and number of copies required. Field-installable ink jet mechanism (top) outputs up to 300 char/s with low noise; the needle mechanism (bottom) produces 90 char/s and multiple copies





Producing sufficient character density for use in printing bar codes, the Centronics 306 SC incorporates a dot matrix mechanism such as that shown at top. Tally's T-1612 teleprinter incorporates a printhead (bottom) that positions needles and coils for maximum straight line design, because needle wear increases proportionally to curvature

Using the 12-needle printhead, the unit outputs up to 90-char/s on an original and up to three carbon copies. Characters are represented in a 12 x 9 dot format; 9 x 9 dots are used for printing capitals and lower case letters, the other 3 x 9 dots allow the descenders of lower case letters to be formed below the line for legibility. Ink ribbon is contained in a cartridge and has a printing life of 4 x 10^6 characters; useful life of the needle printhead is equivalent to 100 x 10^6 characters.

For use where low noise, high speed operation is an asset, the ink jet printing mechanism forms the same 12 x 9 dot characters, by means of 12 jets in two vertical rows at a <35 dB noise level. Individual droplets of ink form up to 300 char/s, printing back and forth across the

YOU CHOOSE THE WINNER

PROCESSOR	6/16	NOVA 3/4	PDP-11/04
Data Type Lengths (bits)	4,8,16,	16	1,8,16
Instruction Word Length (bits)	16,32	16	16,32,48
General-Purpose Registers	16	4	8
Hardware Index Registers	15	2	8
Maximum Memory Available (KB)	64	64	56
Directly Addressable Memory(KB)	64	2	56
Automatic Interrupt Vectoring	Standard	N/A	Standard
Parity	Optional	Optional	N/A
Cycle Time (nanoseconds)	600	800	725

PRICE	6/16	NOVA 3/4	PDP-11/04
8KB Processor	$2200	$2600	N/A
16KB Processor	$2800	$3200	$3795
32KB Processor	$4000	$4400	$4995
Multipy/Divide Hardware	$ 950	$1400	$1820

Interdata's 6/16 wins the battle of the specs.

Not only do we cost less than the Nova 3/4 and the PDP-11/04, we have more features. Just compare: 16 general purpose registers on the 6/16 to simplify programming and reduce fetches . . . only 4 in the Nova and 8 in the 11/04; 15 hardware index registers on the 6/16 against 2 for the Nova and 8 for the 11/04; 64 KB of directly addressable memory instead of just 2 KB for the Nova 3/4 and 56 KB for the PDP11/04.

What's more; all these hardware features enhance the nimble 6/16's performance. Its cycle time is only 600 nanoseconds, compared to 800 for the Nova and 725 for the 11/04.

Interdata's comprehensive software drives this powerful hardware full out. You get the field-proven OS/16 MT2, a real-time, multi-tasking operating system providing instantaneous response to events, while allowing the user to minimize memory by storing non-critical functions on disks. And the 6/16 can be programmed in your choice of FORTRAN, BASIC or MACRO CAL.

All this and save money too, as much as one-third less than a PDP-11/04 and substantially less on a Nova 3/4 . . . with OEM discounts saving even more.

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CIRCLE 23 ON INQUIRY CARD

page. In addition to speed, this technique offers the benefits of no mechanically moving parts, and virtually unlimited service life. Ink supply is sufficient for printing 5 x 10^6 characters.

The terminal transmits characters in bit-parallel or bit-serial form. Bit-parallel data transmission allows optimum use of printing speed; bit-serial transmission adapts to telegraph speeds up to 300 baud (up to 600 baud in special cases). Automatic operation is provided by adding paper tape or magnetic tape units.
Circle 141 on Inquiry Card

A keyboard teleprinter, available in RO and KSR versions, the 132-col model T-1612 matrix impact printer can communicate at line rates from 300 to 9600 baud, and sustains a full 1200-baud line rate when printing. Incorporating the T-1000 series bidirectional printer, the unit is rated at 160 char/s, and uses an internal microprocessor to compute the shortest distance to the next print position.

Tally Corp, 8301 S 180th St, Kent, WA 98031 designed the unit to serve both interactive console and communications applications, eliminating the need for having a console teletypewriter and separate output printer. Its internal microprocessor allows the operator to control the interface for half-duplex, full-duplex, and echoplex operation. It also selects ETX, EOT, or reverse channel protocols, as well as attended or unattended operation, and local or remote communications.

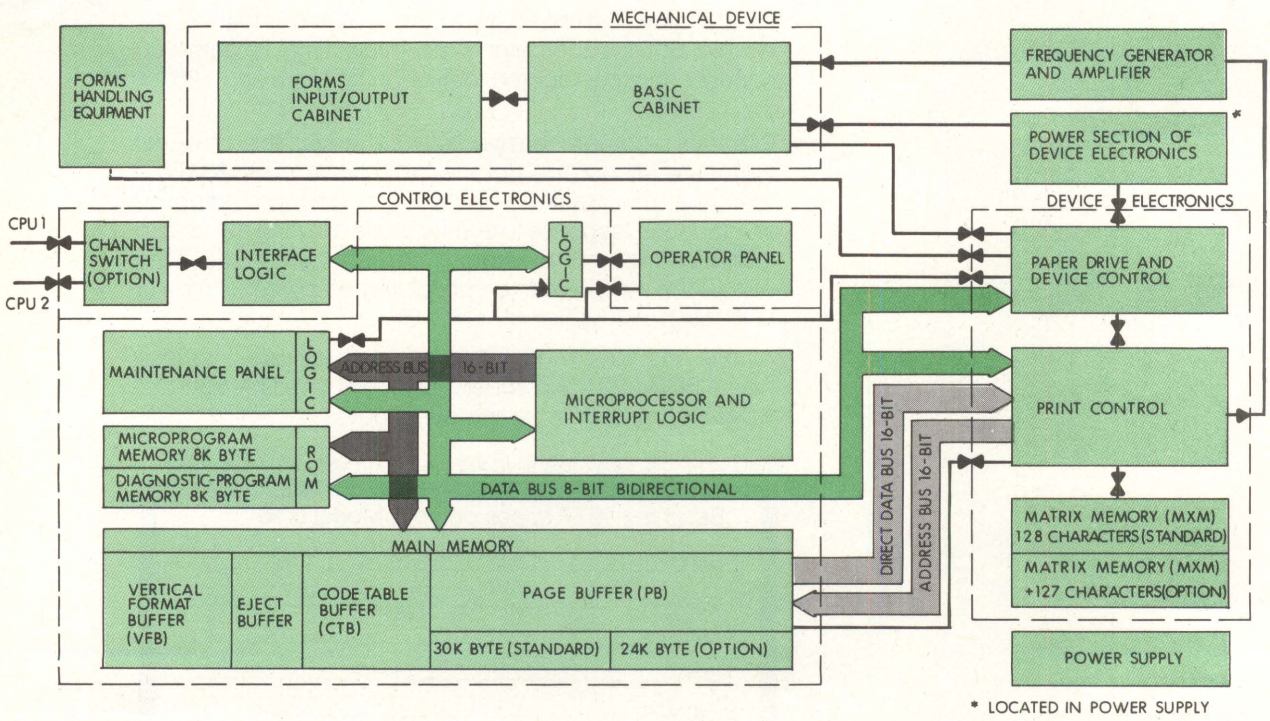
Mechanical and electronic design techniques reduce moving parts and increase operating efficiency. Printhead movement is controlled by a stepper motor for positive positioning and fast response. Two rails hold the printhead carriage in exact alignment to achieve precise alignment. Dual tractor engagement above and below the printline assures positive alignment and rapid paper advance.

With prices starting at $3490, the unit uses a 7 x 7 half space matrix font for sharp definition of its 96 printing characters on an original plus five copies. Noise level is rated at <55 dB.
Circle 142 on Inquiry Card

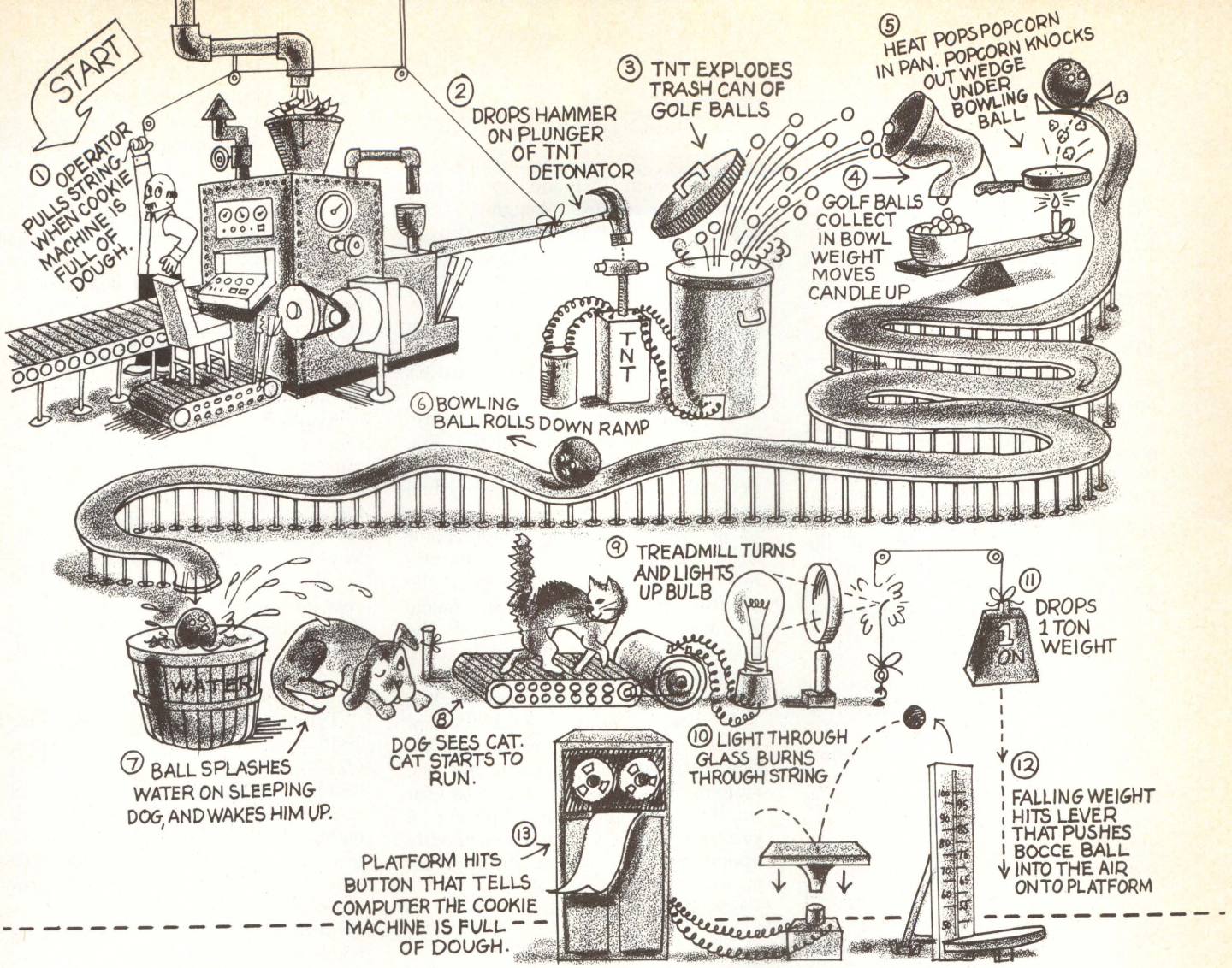
Special-Purpose Units

Two dot matrix printers serve to illustrate how certain features can be used to fulfill the needs of specialized applications. Developed by Centronics Data Computer Corp, Route 111, Hudson, NH 03051, the 306 SC is capable of providing sufficient character density for use in printing bar codes. With a single unit price of $3950, the unit also prints alphanumeric characters, symbols, and contiguous horizontal and vertical bars. It can produce lines of characters from 0.1″ (2.54 mm) high to newspaper headline size at from 100 to 165 char/s. The number of characters to be printed on a standard 8″ (20.3-cm) line can be selected via program control or through use of an optional manual selection switch.

Filling needs for five or more high quality copies in areas such as ticket printing, invoicing, inventory control, and traffic management, where thick forms and/or high quantity distribu-



Microprocessor-based control electronics handle data transfer, page buffer loading, and printing system functions of the Siemen's nonimpact ND2 printer. Unit uses laser technology and an electrophotographic printing method to produce 21,000 lines/min on ordinary computer paper



How to avoid the interfacing nightmare.

If you've got a computer, the easiest way to avoid the kind of nightmare interfacing can become with *anybody's* machine is to simply come to us—the world's largest supplier of interface modules.

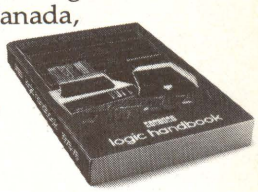
Besides being number one in sheer volume, we're also number one in technology. With a new line of microcomputer products for the LSI-11: A DMA module, an expansion backplane that doubles card capacity, and a foundation module for custom interfacing. Plus a new line of high density wire wrap cards for our larger machines. All part of our substantial library of off-the-shelf solid state modules and compatible hardware featuring the best cost-performance ratio in the business.

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And turn it into one sweet dream.

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CIRCLE 24 ON INQUIRY CARD

tion of reports are required, the 306 TP produces clear, readable copies on multipart forms up to 0.030″ (0.762 mm) thick. It has a single unit price of $2280.
Circle 143 on Inquiry Card

Ultra High Speed Units

In the high performance area, the nonimpact ND-2 generates characters with a laser beam character generator and transfers them electrophotographically onto ordinary computer paper. Introduced by Siemens Corp, 3 Computer Dr, PO Box 5006, Cherry Hill, NJ 08034, the unit operates online with a mainframe in the Siemens 7000 series class, handling data line by line and printing page by page, to output 21,000 lines/min.

Data transfer, page buffer loading, and printing system functions are controlled by integrated microprocessor-based control electronics. Each write command enters one printline in the page buffer. When enough information has been transferred to form a complete page of output, the actual print operation takes place, independent of the CPU.

The unit uses laser technology and an electrophotographic printing method. A rotating drum with a photoconductive surface is electrostatically charged. Print information is placed on the drum in the form of charge patterns by means of exposure with a laser beam. In the developing station, toner particles adhere to the exposed positions in accordance with the charge patterns. Paper to be printed is fed past the drum, and the toner particles are transferred from the photoconductor to paper in the transfer station, then are fused into the paper by means of heat and pressure in the subsequent fuser station.
Circle 144 on Inquiry Card

A similar unit from Xerox Corp, Data Systems Div, 701 S Aviation Blvd, El Segundo, CA 90245, the 9700 Electronic Printing System operates from IBM computers in the /360 or /370 class or from magnetic tape units. This xerographic printing system generates forms and symbols as well as type fonts and sizes, and is capable of continuous operation, printing on plain 8.5 x 11″ (21.6 x 28 cm) paper at 2 pages/s or up to 18,000 lines/min. High print quality is achieved with a resolution of 90,000 dots/in^2.

The system is made up of four subsystems: control, imaging, xerographic, and output. Control subsystem includes an internal computer with up to 128k bytes of core storage, a disc drive with capacity for approximately 26M bytes, a character dispatcher, output device controller, and the keyboard/display operator's console.

Incoming information is preprocessed, then buffered on the disc. A pattern of modulated laser light generated in the imaging subsystem creates a latent image of the page to be printed on the photoreceptor belt. Paper from the input stations moves in a straight path past the photoreceptor belt, where the image is transferred to paper, through the fusing area, where charged toner particles are fixed permanently to the paper, and on to the output stacker.

Keyboard/display unit at the operator's console permits communication between the operator and the system. The operator may ask for duplicate sample copies during a printrun, and may initiate and modify operations. The screen displays instructions for the operator.
Circle 145 on Inquiry Card

Computer Processors Demonstrate Ability to Perform Mix of Tasks

Offering field-upgradable growth from existing 1600 family processors, 1650, 1660, and 1680 processors offer concurrent multifunction capabilities to users trying to sort out distributed vs nondistributed, and remote batch vs interactive applications. Harris Corp's Data Communications Div, 11262 Indian Trail, PO Box 44076, Dallas, TX 75234 claims that operating systems and communications facilities allow the systems to integrate batch and interactive hardware and software into a single centralized controllable system.

The 1650 processor, with memory expandable up to 98,304 bytes, can operate up to eight key entry terminals concurrently with remote job entry communications to central host computers. It is intended primarily for concurrent remote batch/key disc data entry applications. The 1660 is capable of performing a variable mix of remote job entry, batch COBOL, key entry, and interactive applications. A dual-processor configuration, the 1680, enables users to combine any two family members into a single unit having combined capabilities of the individual systems.

In addition to interactive CRT/key entry devices, the machines support a full line of peripherals. Depending on configuration, the processors offer up to four synchronous communications channels, 15 asynchronous interactive channels, three direct memory access channels, and a multiplexed channel for a variety of standard I/O devices.

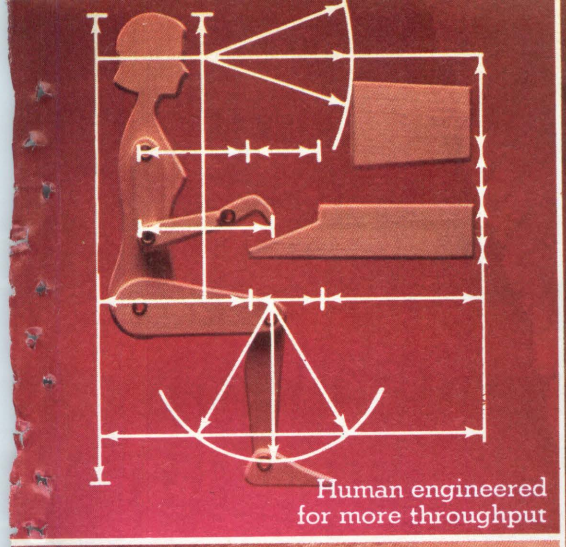
Available software includes emulation packages to support remote communications with various mainframes, plus interactive and batch languages for local processing, inquiry, data entry, or file update complications. Key-disc software packages—Format/10 and /41—enable a system to process intermixed format- and program-driven applications. Since no knowledge of programming is needed to use them, they can be implemented by keypunch supervisors.

Typical of the price range are: 1650, including four key stations, 65,536-byte memory, 6M-byte disc, 300-line/min printer, and 9600-baud communications, $60,720; 1660, with eight CRT keystations, 98,304-byte memory, 12M-byte disc, 1200-line/min printer, and 19,200-baud communications, $128,888. Pricing for the 1680 depends on the processors being combined and the configuration.
Circle 146 on Inquiry Card

Shared Architecture Multiprocessor Meets Critical Networking Needs

Offering dual processors with dual cache bus and 500k bytes of error correcting memory, the GA-16/550 multiprocessor system provides mainframe power with minicomputer size and economy. The system's shared architecture is claimed by General Automation, Inc, 1055 SE St, Anaheim, CA 92803 to yield high throughput, increased system integrity, and fail-safe redundancy—all necessary to networking applications.

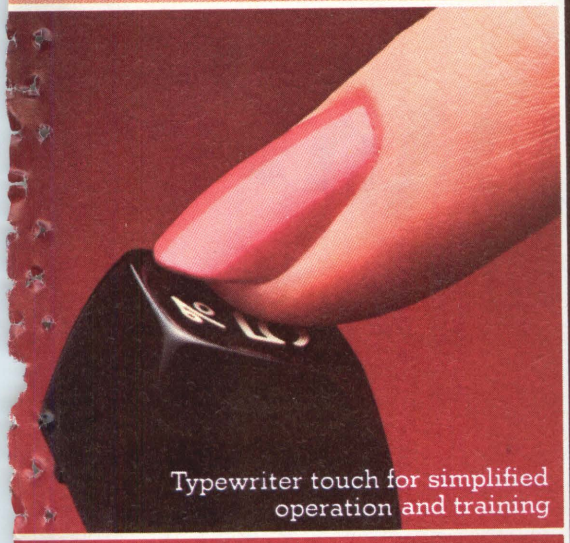
Critical system element is the dual cache bus structure connecting up to eight high performance processors to a large shared memory facility. A single bus can transfer data between as many as four processors and four memory banks at rates up to 8M bytes/s. Integrity of data transfers is protected by a parity per byte system. Since the bus can be accessed



Human engineered
for more throughput



Reduced glare, reduced eyestrain



Typewriter touch for simplified
operation and training



State of the art technology
with a human touch.



THE MOST SOPHISTICATED, COMPLICATED COMPONENT OF ANY DATA TERMINAL SYSTEM IS THE PERSON BEHIND THE CONSOLE.

When we designed the Teletype® model 40 product line, we paid as much attention to human engineering as we did to electronic engineering. Simply because we don't think one makes much sense without the other.

After all, throughput is as much a function of operator performance as it is of advanced CMOS technology.

That's why we positioned the tube so it's a comfortable 19" to 21" from the operator. The tube isn't in a fixed position, either, but tilts through 20° to adjust for lighting conditions and individual viewing preferences.

To eliminate eyestrain, a specially darkened and etched glass is used on the screen to diffuse surface reflections and increase contrast by 100%. Even the large 7 x 9 display font is designed for legibility, with a flicker-free refresh rate of 60 times/second. Plus generous spacing between characters and lines increases readability even more.

Keyboard controls aren't just grouped by function so they look right, we made them "feel" right, too. Not only do they fit the fingers, they also duplicate the touch and feel of office typewriters.

As you can see, we think the best way to impress you with our model 40 product line is to make sure your operator is impressed. For more information, write: Teletype, 5555 Touhy Ave., Skokie, IL 60076. Or call: 312/982-2000.

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CIRCLE 25 ON INQUIRY CARD

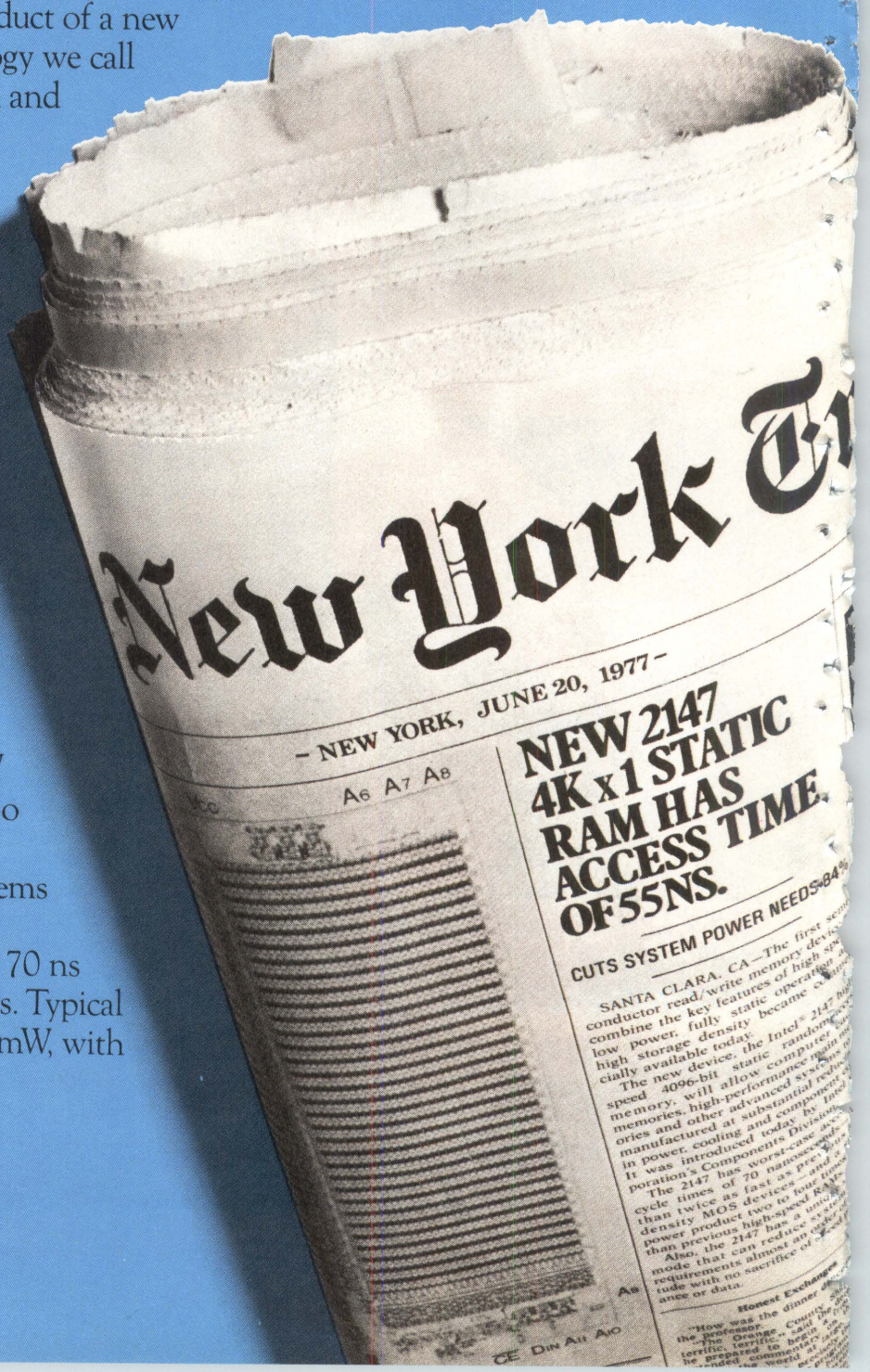
Intel delivers the 2147. memory technology

Imagine a 4K fully static RAM that runs at bipolar speed yet cuts power consumption dramatically, all in a standard 300-mil wide 18-pin DIP.

That's the new 2147. It's a product of a new High-performance MOS technology we call HMOS. The 2147 is in production and we're delivering it now. HMOS makes it a new industry standard in high speed, high density memory. It's sure to change the way you design high performance memory systems.

In fact, the larger the cache, main or add-on memory your design needs, the lower the power consumption per bit with the 2147. A unique new power-down mode makes that power reduction possible. When the 2147 is deselected it stands by at a typical power dissipation of 50 mW —less than 15 microwatts per bit. So you can achieve major savings in cooling and power supplies, in systems large or small.

Access times range from 55 to 70 ns maximum with identical cycle times. Typical operating power dissipation is 500 mW, with



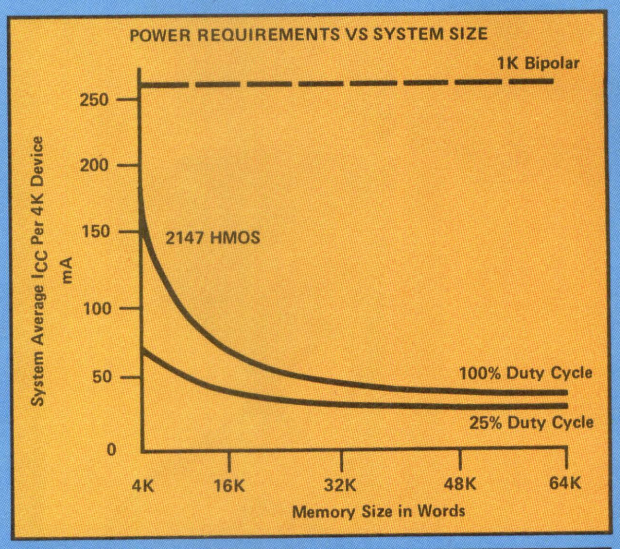
It's HMOS, the new that scoops bipolar.

worst case specs not much higher.

Throughput is always high because the 2147 can respond to select inputs as fast as to address inputs. HMOS eliminates the power-up delays of conventional power-down techniques.

On top of this the 2147 is fully static, eliminating the complications of conventional high density RAMs, such as clocking, address set-up or hold times. The 2147 operates on a single +5V supply and is directly TTL compatible. It uses the industry standard pin-out for 4K x 1 static RAMs. The chip itself measures only 158 mils square.

Now Intel has an expanded family of HMOS 1K and 4K high performance static RAMs: the recently introduced 2115A/2125A and now the 2147. Check 2115A/2125A and 2147 performance specs at right.



HMOS RAMs

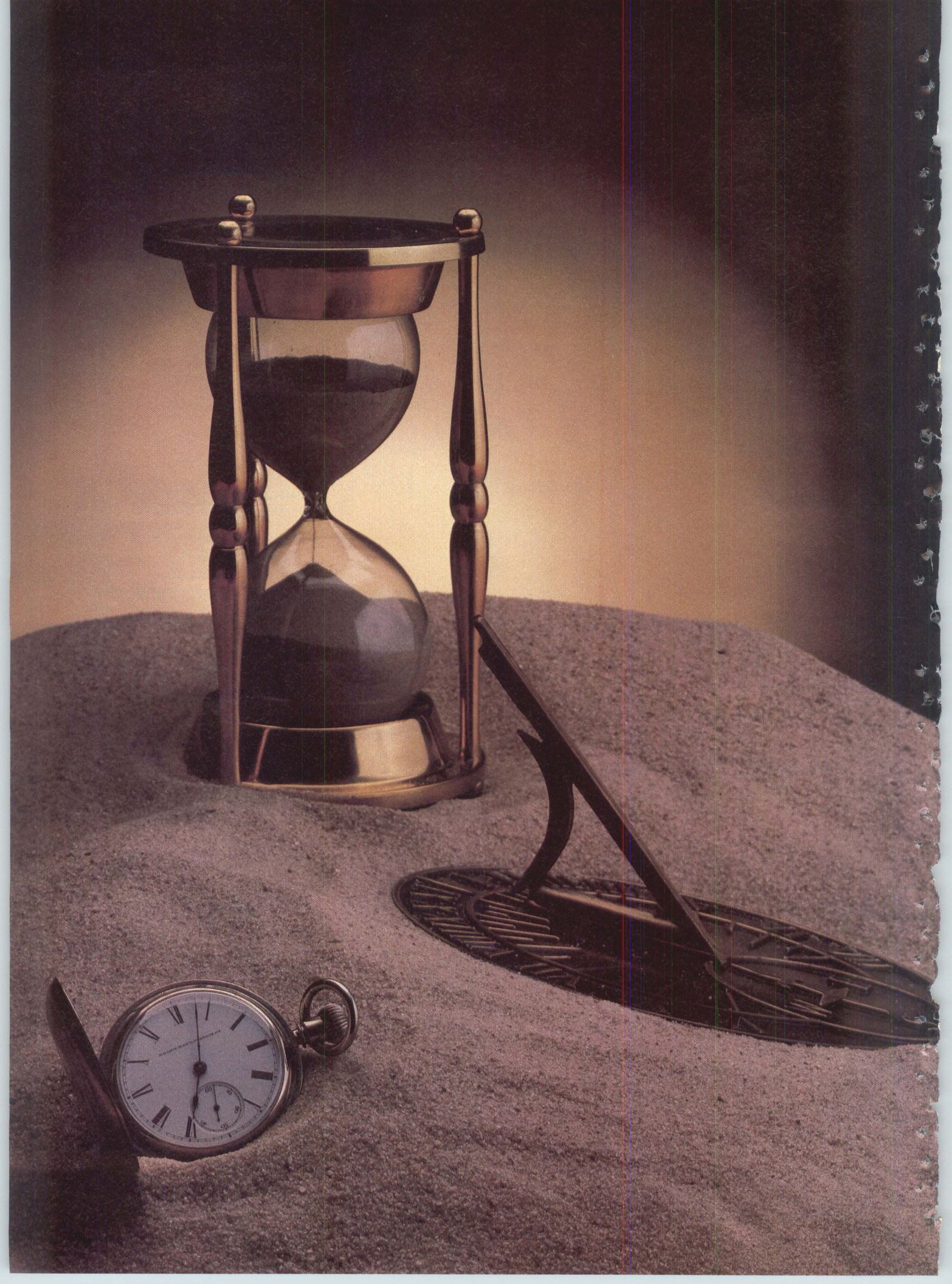
	Density	Current (mA)				Access Time(ns)
		Active		Standby		
		Typ.	Max.	Typ.	Max.	Max.
2147	4K	100	160	10	20	70
2147-3	4K	120	180	15	30	55
2115A/25A	1K	100	125	N/A		45
2115AL/25AL	1K	60	75	N/A		45

Order 2147's, 2115A's and 2125A's from your local Intel distributor. Contact: Almac/Stroum, Component Specialties, Cramer, Hamilton/Avnet, Harvey Electronics, Industrial Components, Pioneer, Sheridan, L.A. Varah, Wyle Liberty/Elmar or Zentronics.

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Look into the operating systems, the languages, the data base system, the real-time device handlers and terminal systems, and you will see that we build for the real-time environment. That's our business.

Choose from a well-bred family of computing systems: The SEL 32/35, the SEL 32/55, or the SEL 32/75. Unlike other so-called "32-bit minis" that are only bridge-the-gap systems developed from essentially 16-bit architecture, all SEL 32 systems are true 32-bit machines. This results in richer instruction sets, more precision in data representation and larger, directly-addressable memory. All are available with throughput rates in excess of 26 million bytes/second.

Systems computers fit the term "minicomputer" in price alone. If your application is performance-sensitive, we'll save you money. If you're budget-sensitive, we'll give you more performance for your dollar.

The SEL 32/35 can be configured from 64K bytes to 512K bytes of 900 nsec memory. Resembling its more powerful brothers, the SEL 32/35 is a complete package, including control processor with floating-point arithmetic, memory, chassis, power supplies and cabinet.

The SEL 32/55 is offered in a variety of both single and multiple CPU configurations, with from 32K bytes to 1 million bytes of 600 nsec memory.

The SEL 32/75, with up to 16 million bytes of main memory, has a concept so new, we had to coin a special term to describe one of its main features: Regional Processing Units. Working independently, these RPU's contain sufficient control and buffer storage areas to process an I/O region and transfer the resultant data directly to main memory. Computer system throughput is further enhanced by High-Speed Floating- Point Hardware and Writeable Control Storage.

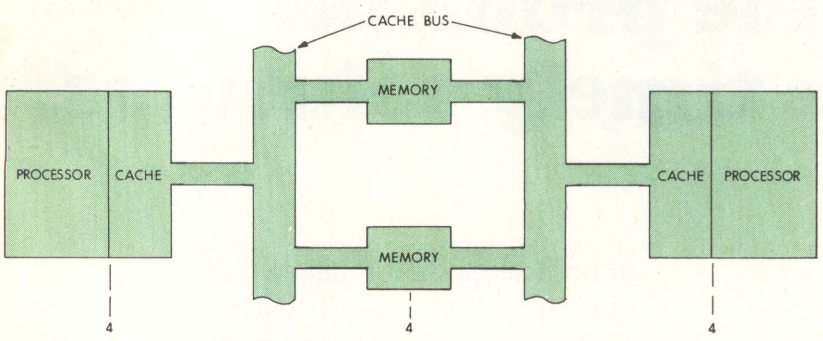
Just circle our number on the Reader Service Card, or call us today. We'll send you the powerful story of the SEL 32 family.

SYSTEMS
ENGINEERING LABORATORIES

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CIRCLE 27 ON INQUIRY CARD



Dual cache bus structure, central to General Automation's shared architecture 16/550 multiprocessor system, connects up to eight processors to a shared memory facility. A single bus can transfer data between four processors and four memory banks at rates of 8M bytes/s

by the user, it can be used as a special 32-bit input channel for transferring data from high speed peripheral devices directly into main memory.

A microprogrammed computer with a 240-ns microcycle time, the 16/550 has a 2048-byte 120-ns cache memory, 1024 words of 64-bit control store (expandable to 2048 words), repertoire of 145 basic instructions (including 14 byte string and nine decimal arithmetic operations), and a comprehensive memory management system (MMS). MMS dynamically addresses 2M bytes of working memory and provides parity generation and error detection, as well as write-protect and execute-protect for selected blocks of memory.

The system's dual port memory system is organized 4 bytes wide with complete 7-bit check codes, which detect and correct all 1-bit errors and detect all 2-bit errors. Memory is available in 128k-byte increments, implemented using HYPAK high density semiconductor memory modules. The modules use hybrid technology to reduce both the size and cost of memory. A single DIP contains 32k bits or 4k bytes, twice the capacity of other memory chips. This increase in capacity reduces the number of memory assemblies necessary for 128k bytes from eight to three. In addition to reducing the size, the modules enable error correction capability to be incorporated while maintaining a significant decrease in cost.

Software support is provided to the system in the form of Control, a foreground/background multiprogramming operating system; four language processors including FORTRAN IV, COBOL, Commercial FORTRAN, and MacroAssembler; and a comprehensive ISAM file management system.

Circle 147 on Inquiry Card

Computer Uses 16k RAMs To Pack 1M-Byte Memory In 12.25″ High Package

A high density memory module containing 128k bytes of semiconductor memory and a fault-control memory system are claimed to be the first commercial equipment using 16k-bit, n-channel MOS RAM chips. These memory enhancements, used in combination, have made it possible for the Data Systems Div, of Hewlett-Packard Co, 1501 Page Mill Rd, Palo Alto, CA 94304 to package 1M bytes of main memory with a 21MX E-series computer in a unit only 12.25″ (31.12 cm) high.

The 16k RAM chips are pin-compatible with the 4k RAM devices used on standard memory boards, allowing the amount of memory on each board to be quadrupled. They are sealed in ceramic packages, enabling memory systems to meet environmental specifications that are unusual for computer equipment—an operating temperature range of 0 to 55°C and 20 to 95% relative humidity at 40°C.

Consisting of a memory controller and two check-bit array boards, the fault-control memory system automatically corrects all single-bit errors, and detects and reports all double-bit errors as well as most errors of three bits or more. Fault control permits programs to continue even if a memory module is malfunctioning; the computer will continue to operate even if a memory chip is removed from the board. Since maintenance may be performed on a scheduled rather than an emergency basis, downtime is reduced. Failures are pinpointed at the chip level by fault-indicating LEDs built into each array board.

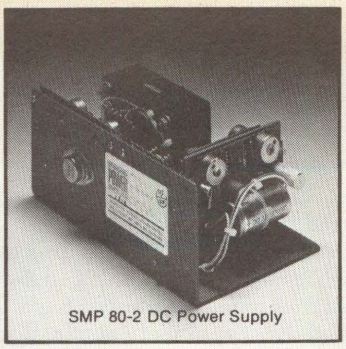
One check-bit array board supports up to 256k bytes; the other to 512k bytes. The boards execute a sophisticated 22-bit Hamming error correction code. Five check bits are appended to the 17 bits on the memory module to form a 22-bit word. The Hamming code is compared to the code stored in memory during each access. Based on that comparison the controller corrects or reports the error.

Packaged with the processor having up to 14 fully powered I/O slots, the computer forms a reliable system that needs no air conditioning and occupies little space. Large memory allows programs to be entirely memory-resident, eliminating swaps from disc as well as the preventive maintenance associated with discs.

RADC calculations and reliability tests indicate that MTBF for 21MX computers is increased ten times by use of the fault control memory. Expected MTBF for the processor and fully incremented memory is approximately 6000 to 8000 hours.

List price for the 128k-byte memory module is $6400. Fault-control memory controller has a price of $600, and associated check-bit boards sell for $2750 (for memory blocks up to 256k bytes) or $5000 (for 512k-byte blocks). A typical configuration, consisting of a 21MX E-series computer with 512k bytes of memory, measuring 8.25″ (20.96 cm) high is priced at $36,000. A 12.25″ (31.12 cm) high unit with 1024k bytes sells for $59,800.

Circle 148 on Inquiry Card



SMP 80-2 DC Power Supply

When you have to engineer for microprocessor-based systems

Our new SMP Series DC power supplies is just the ticket you need for those tough microprocessor-based system applications. And there are several reasons.

First, it interfaces *directly* with the power requirements of virtually all microprocessor ICs. No expensive custom design work is needed.

Too, you can get four independent and isolated outputs. You can power logic, memory and displays, for example, from one simple power source.

For extra flexibility, we give you 115/230 V ac universal input. And we've designed in all the little extras for top performance: well regulated, overvoltage protection, highest quality components and low ripple.

Our SMP 80-2 also features temperature compensated circuitry. So if the temperature goes up, your output stays right on track.

But most importantly, it embodies a reliable design proven in more than 10,000 units now in use.

For specs, price schedule, and product arrival times, telephone your local stocking distributor, or contact Standard Power, Inc., 1400 S. Village Way, Santa Ana, CA 92705, (714) 558-8512. ***Send for new 32-page catalog.***

STANDARD POWER

See us at WESCON '77, Booth 1530

CIRCLE 28 ON INQUIRY CARD

Multilevel Programming Language Upgrades Minicomputer Performance

Reducing application development time, and memory requirements, miniFORTH™ is a standalone multilevel programming language and operating system that produces minicomputer performance comparable to that of larger machines using conventional software. The language, developed by FORTH, Inc, 815 Manhattan Ave, Manhattan Beach, CA 90266, is fundamentally interactive, structured, multilevel, and extensible. Its operating system includes assembler, compiler, interpreters, multiprogrammer, device drivers, virtual memory, data base management, and editing capabilities; all reside in less than 4.5k words of memory.

The reduced number of program statements and the efficiency of interactive programming and testing cycles increase programmer productivity. Unlike other interactive systems, however, the high level system runs only 20% slower than assembler. An interactive macroassembler incorporated in the system allows programmers to access full computer capabilities. This eliminates the need for large assembly language subroutines in a real-time environment, moving users closer to the hardware interface.

The system is currently available for the PDP-11, NOVA, and other CPUs. Minimum hardware configuration is 8k words of memory, disc, and terminal. The standard package is licensed for $10,000.

Circle 149 on Inquiry Card

Small Business Computer Increases Processor Speed To Improve Response

Video-terminal controlled, real-time disc based systems, System Ten 220 Series computers feature increased processor speed, improved disc handling facilities, greater core capacity, and more flexible storage. Introduced by ICL, Inc, Turnpike Plaza, 197 Hwy 18, East Brunswick, NJ 08816 (result of the integration of Cogar Corp, a subsidiary of Singer Business Machines, with International Computers USA Ltd), the machine is compatible with System Ten, offering existing users an opportunity to expand or upgrade.

Heart of the system is a processor which can handle up to 20 different operations simultaneously. Each operation is controlled automatically. Information is entered via a visual display terminal, which is also used to prompt the operator. Each entry is checked as it is made, assuring an accurate data base.

The model 22 processor has a 33% improved memory cycle time to provide faster response to inquiries, and faster turnaround on jobs. Maximum memory size is 160k characters, increasing the user partition size from 10k to 80k characters and the common core size from 65k to 80k characters to provide more efficient program writing and execution.

Processor consists of up to 20 fixed hardware partitions; the number of partitions is determined by the number of jobs or users; the size of each is determined by the application to be run. To service requests and keep track of partitions, the processor provides automatic hardware controlled multiprogramming, by switching control to each partition in turn for a limited period.

In addition to processor, CRTs, and printers, the system incorporates disc storage, and can use magnetic tape for supplementary storage. The system's model 43 fixed/exchangeable disc drive has capacity for 8M characters and a seek time almost twice as fast as its predecessors. A 20M-character disc drive, model 44-3, is available as an alternative. Disc or tape units are connected to the processor through a file access channel. One channel accommodates up to 10 disc drives and up to four magnetic tape units.

System support is provided by an improved disc management system (DMF2), assembler, sort, and RPG II. Application packages are available for accounting, sales order processing, and payroll, as well as more specialized packages.

Circle 150 on Inquiry Card

Software Extends Autointeractive Concept to IC Design Development

Extending the concept of autointeractive design to the development of integrated circuit design, the Microcircuit Design Package reduces design time by half. Announced by Redac Interactive Graphics, Inc, 225 Great Rd, Littleton, MA 01460, the software, incorporating automatic design aids, runs on a Digital Equipment Corp, XVM computer graphics hardware configuration.

The package can be used for IC design in all technologies including bipolar and MOS. A designer works with the XVM system using a lightpen on a 21" (53 cm) refreshed display graphics terminal. Automatic aids include cell placement, metallization routing, and design-rule checking routines.

A multitasking package is also available, which permits two graphics terminals to operate simultaneously from the same computer system. For use with Design-A-Matic or equivalent configurations, the multitasking package will permit full IC and IC design to be executed on one system. The combination can result in a fully integrated design effort.

Circle 151 on Inquiry Card

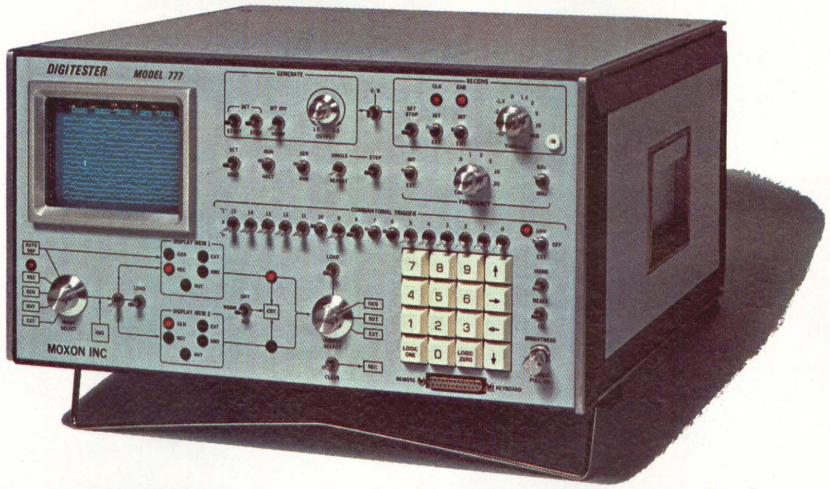
LSI Test System Incorporates Local Memory To Speed Throughput

Increasing production test throughput as much as 200%, the Sentry v, a low cost, automatic test system, serves to substantially reduce per device testing cost. The system, introduced by Fairchild Camera and Instrument Corp, Instrumentation and System Group, 1725 Technology Dr, San Jose, CA 95110, will handle n-MOS, p-MOS, CMOS, ECL, TTL, and IIL technologies.

Based on a 24-bit CPU, the system consists of 30-pin test station, from 32k to 196k words of local memory, video keyboard terminal, and magnetic tape unit. It handles microprocessors, peripheral chips, bit slices, phase lock loops, RAM and ROM devices, shift registers, universal asynchronous receiver/transmitters, and digital hybrids. Semiconductor memory allows the unit to perform rapid local memory and special processor loading for the actual tests, increasing efficiency by as much as 200%.

Programming costs are minimized by source program compatibility with other Sentry series testers. Hardware

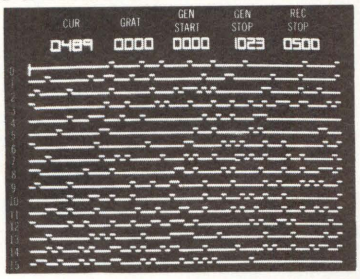
If you're considering a LOGIC ANALYZER or DATA GENERATOR, see the one that's both



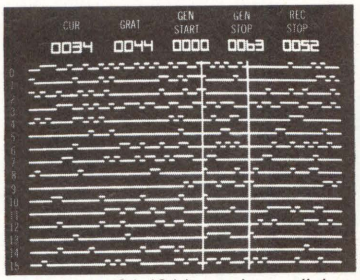
It's a DIGITESTER...3 digital test instruments in 1.

Here are 3 ways you can use a DIGITESTER to reduce your digital logic design costs

INITIAL DESIGN...
It's a DATA/WORD GENERATOR



Generate 1024 serial bits to help you develop your communication products.

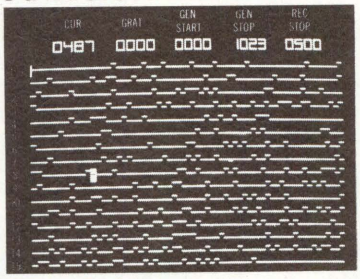


Generate up to 64, 16 bit words parallel so you can test your interfaces.

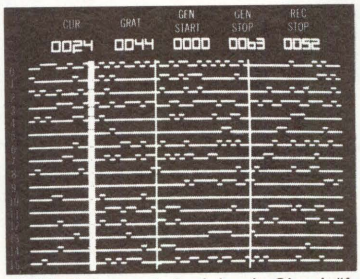
The DIGITESTER Model 777 is the most valuable test instrument you can get for developing or testing digital logic products...including microprocessors.

To begin with, no other test instrument is quite like the DIGITESTER. It offers you unequalled flexibility for simultaneous or independent logic generating, logic receiving/analysis or comparison. Programs are stored in 1 of 4 internal memories, ready for transfer at variable data rates up to 20 MHz, internally or externally controlled.

TROUBLESHOOTING...
It's a LOGIC ANALYZER



Serial look forward–look back lets you see up to 1023 bits on either side of Trigger Point.



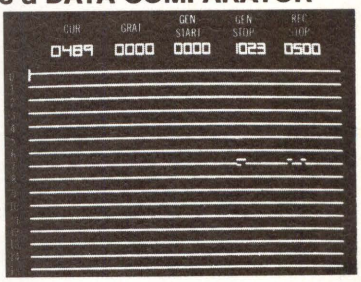
Parallel look forward–look back. Check "fault" symptoms on both sides of selected pattern.

You can generate any program with any number of "1" or "0" bits, by using the integral scratch pad keyboard...or an external source if you prefer.

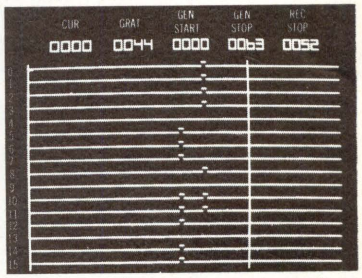
Data is displayed jitter-free, on a 5″ CRT. Cursor, graticule, generator start, generate stop and receive stop positions are numerically displayed on the CRT.

Of course the DIGITESTER has all front panel controls needed to make digital development and test work fast, easy and accurate.

TEST/RECEIVING INSPECTION...
It's a DATA COMPARATOR



Compare serial response with known program in memory and see disagreement appear.



Compare input data with expected pattern in memory and see errors as difference bits.

You get 3 precision instruments in 1 with exceptional versatility for $9495.00.

Contact the factory or your local Moxon sales engineer to find out about all the DIGITESTER'S capabilities and discover the savings you'll accrue compared to home-built pattern generators... plus you'll have the added savings of a logic scope. The DIGITESTER can pay for itself in a year. So be sure you see the DIGITESTER...it's the only one that's both a Logic Analyzer and Data Generator.

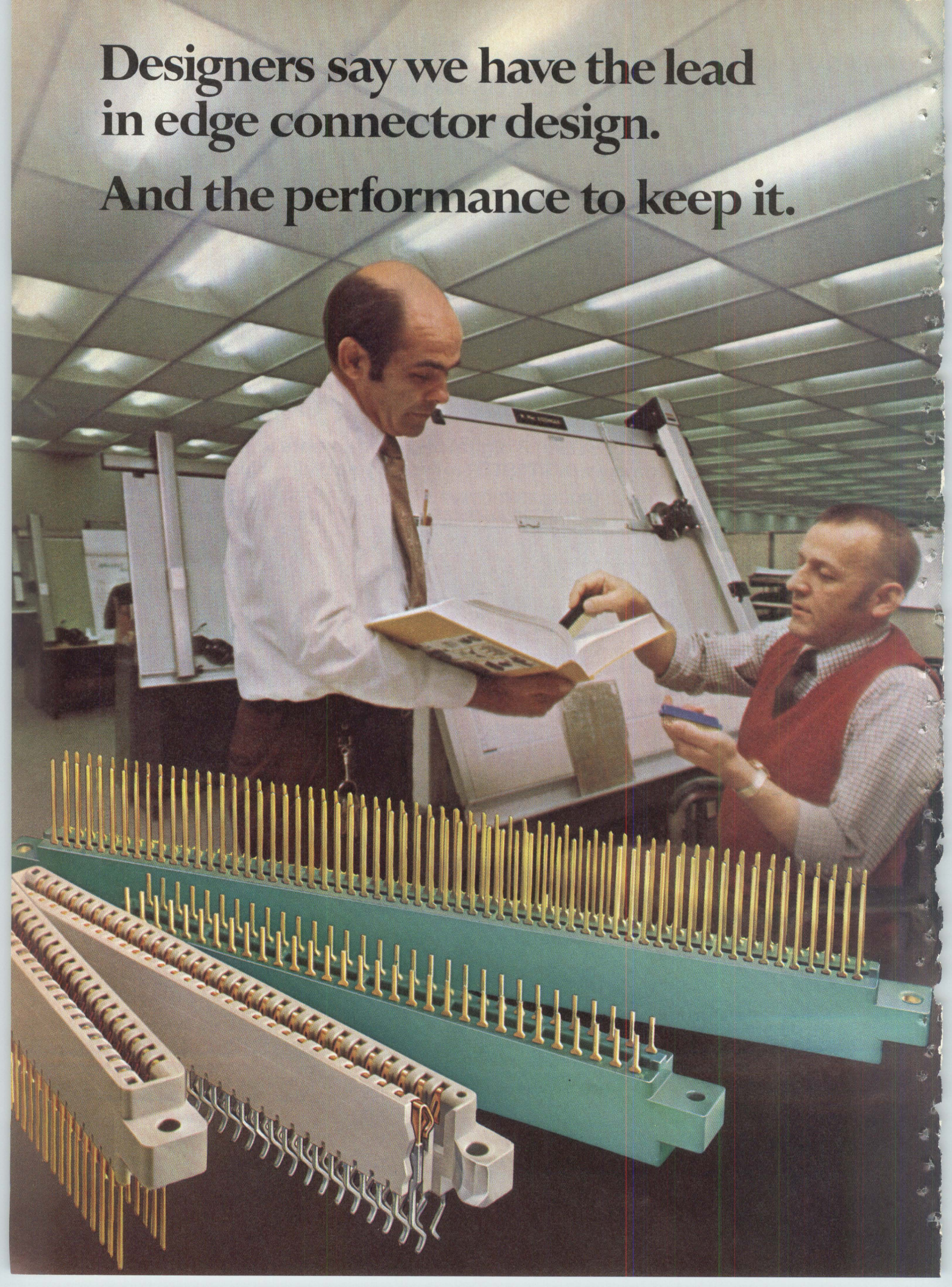
moxon inc.

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CIRCLE 29 ON INQUIRY CARD

Designers say we have the lead in edge connector design.

And the performance to keep it.



The reason why is clear. The contacts for AMP wrap-type edge connectors have unique strength and stress relaxation characteristics that assure long-term top performance. And they come in either leaf spring or cantilever types. Each incorporates full bifurcated design to achieve effective contact redundancy. A choice of contact alloys and selective gold platings is available too. The result is premium reliability and performance at a cost as low as 2 cents a line in quantity.

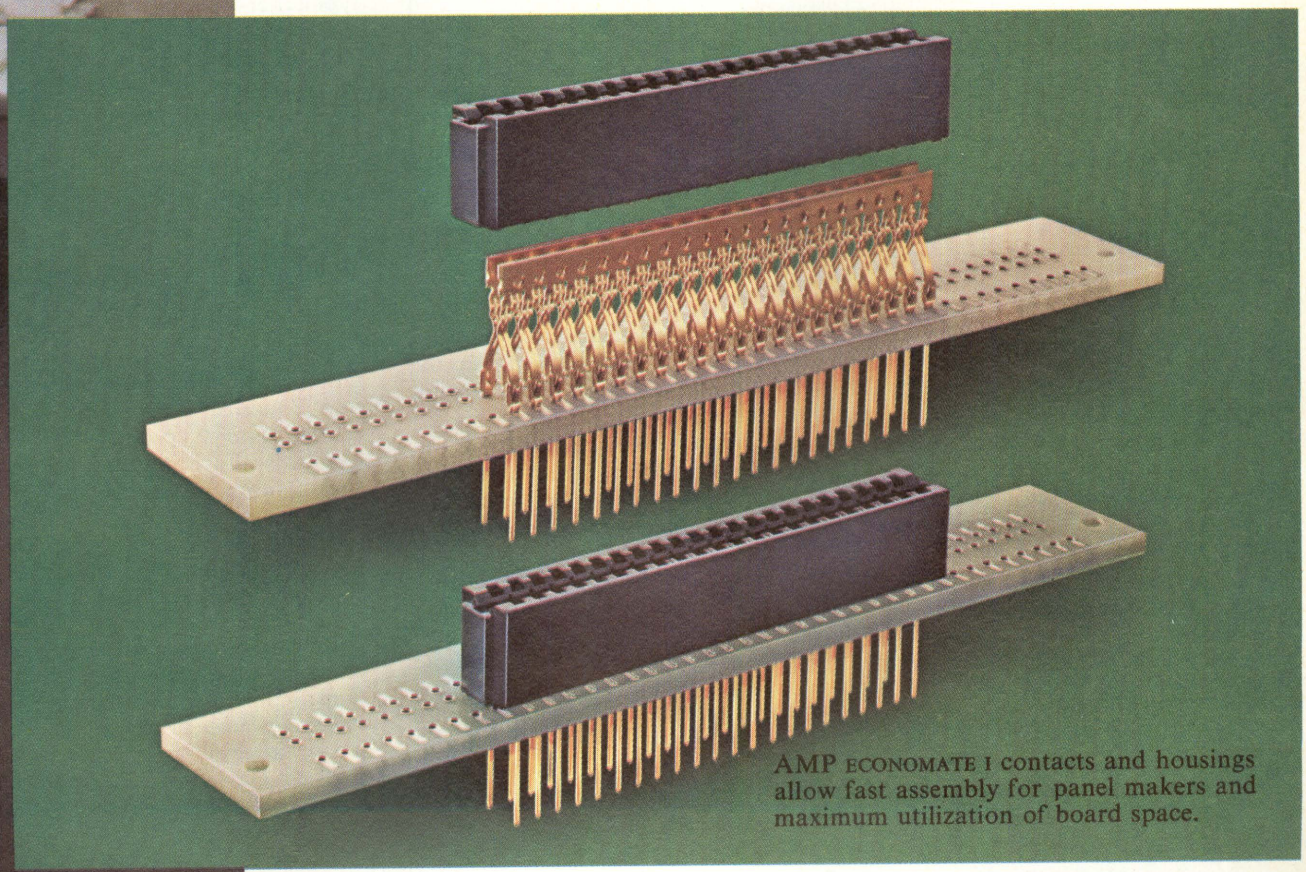
There's another reason you're ahead with AMP edge connectors, or any other AMP product for that matter. It's called technical support. It means you can call on us for assistance in research, product design, and production. We feel the professional engineer is entitled to it. After all, when he puts his confidence in us, we can do no less than back him fully.

There are other advantages, too, with these AMP edge connectors. You can select from types for either rack or solder-to-board mounting. And if you're a panel maker, we've got ECONOMATE I connectors with outstanding insertion speeds and space savings.

For more information on these wrap-type printed circuit edge connectors, just call AMP Customer Service at (717) 564-0100. Or write AMP Incorporated, Harrisburg, PA 17105.

AMP has a better way.

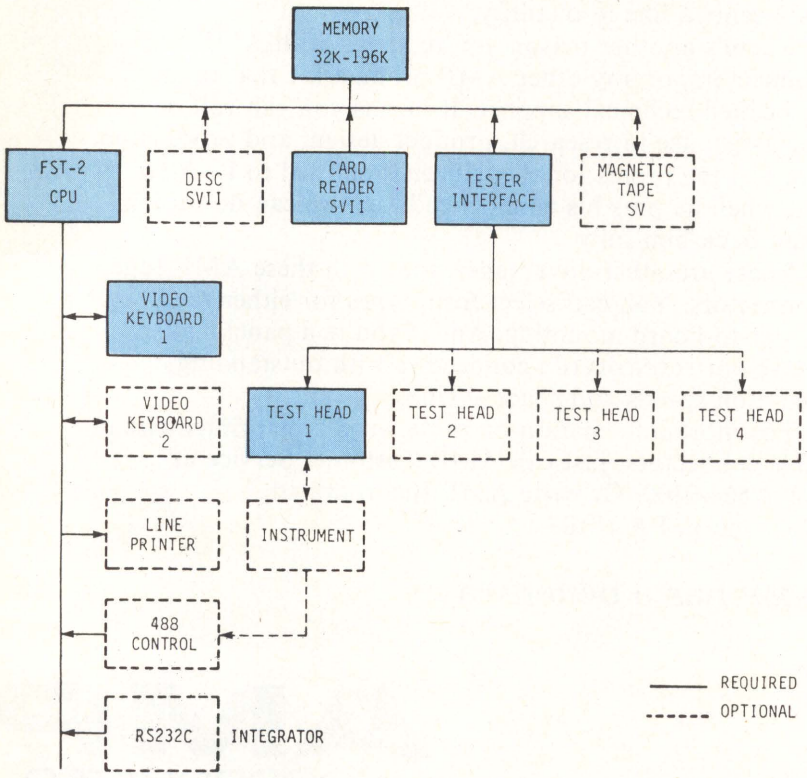
AMP
INCORPORATED



AMP ECONOMATE I contacts and housings allow fast assembly for panel makers and maximum utilization of board space.

AMP is a trademark of AMP Incorporated.

CIRCLE 30 ON INQUIRY CARD



Based on a 24-bit CPU, Fairchild's Sentry V LSI production test system incorporates up to 196k words of semiconductor memory, permitting large increases in test efficiency. Devices handled include microprocessors, peripheral chips, semiconductor memories, and digital hybrids in SOS, ECL, IIL, and other technologies

compatibility with the Sentry VII eliminates correlation problems between engineering and production systems.

Use of enhanced operating systems software permits multitask operation, allowing, for example, testing to progress in the foreground while the primary video keyboard terminal is used to load files into memory or control the data logger. A second operator can simultaneously use the alternate terminal to edit a source program.

Actual test programming can be created through the high level FACTOR language. Users can formulate testing routines in a modular fashion, developing only the macro sequences needed for a specific device or technology. Control programming in the systems software links these macros into a complete program.

Special-purpose modules that operate in a real-time, multiprocessing mode, are available. Of these, the sequence processor handles more complex semiconductor devices such as microprocessors. This module provides the system with the capability to run complete instruction sets, worst case instruction sets, and ac and dc parametric tests, checking voltage margins, verifying 3-state output, and confirming external interrupt performance. Another, the pattern processor module substantially decreases the time required to run test patterns on memory devices to 65k.

The system can access an Integrator via an optional hardwired connection or telecommunications link (RS-232-C). The Integrator processes system output for reformatting into standardized information systems. This link increases efficiency by allowing the removal of the test data processing burden, providing access to massive archival storage of test programs and test data, and transmission of programs and test data generated at one facility to another.

Circle 152 on Inquiry Card

Dispersed Processing System Adds Power and Flexibility

Recent addition to the family of dispersed data processing and business computing systems produced by Datapoint Corp, 9725 Datapoint Dr, San Antonio, TX 78284, the 6600 Advanced Business Processor offers 120k of user memory, advanced memory space handling, and an enhanced instruction set. The unit includes a typewriter-style keyboard, 11-key numeric pad, video display, and dual cassette tape decks. It is designed for use with disc-based systems.

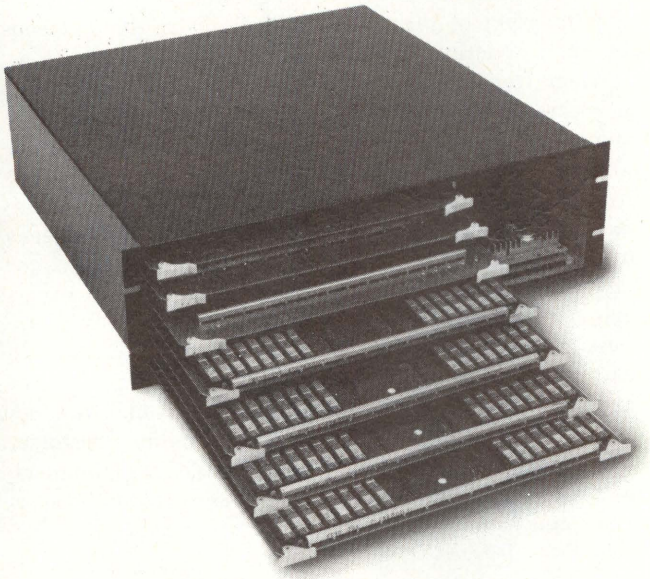
The processor has a 16-bit wide internal architecture and 600-ns memory cycle. Its extended instruction set has been enhanced to increase throughput in sophisticated configurations, and includes 8- and 16-bit manipulations, hardware multiply/divide, and list handling instructions.

Used as a host computer for the multitask, multiuser Datashare® Business Timesharing System, the processor can support up to 24 video display terminals. Each terminal can direct execution of the same or different programs concurrently. With memory partitioning software, both timesharing applications and batch programs to remote sites can run simultaneously.

Included in the library of compatible software supporting the machine are tape and disc operating systems; emulators; and general business languages such as COBOL, RPG II, and BASIC; as well as special languages such as Datashare, Databus®, Multilink™, and Dataform®. □

Circle 153 on Inquiry Card

512K x 22 and you'll love every bit of it.



It's a lot to love . . . a whole megabyte of memory in one teeny 5¼x 19 inch box.

How could we do it?

16K RAMs.

That gives our new NS-3 memory system more memory in less space than you could ever get before in a standard memory system.

Besides, all the things that made you know and love our old NS-3 are still there to know and love.

Access time up to 250 ns, cycle times as fast as 500 ns, low cost, the flexibility of being able to select word length, larger chassis for more capacity, error correction, parity generation, double word control, custom interface, etc.

You can even get NS-3 with 4K RAMs.

Just in case 512K x 22 is a bit too much for you to love.

CD-8

National Semiconductor
2900 Semiconductor Drive, Santa Clara, CA 95051.

Please send me further information about your NS-3 memory system.

Name_____

Company_____

Address_____

City_____ State_____ Zip_____

National Semiconductor Memory Systems

DIGITAL CONTROL AND AUTOMATION SYSTEMS

Automated Updating Gives Security Trading Firm Constant View of Inventory

When an average security processing transaction is about $2 million and when major purchases are financed, it is essential that updated inventory information be available constantly for management decisions. Important factors in maintaining profitability of the trading company are limiting these financing costs as well as reducing the cost of adding personnel in periods of company growth.

One Wall Street firm in New York City, A. G. Becker & Co—which in 1975 handled a total of $55 billion in commercial paper (money, bonds, and credit securities) —helps keep these factors under control through use of an online computer system. This comprehensive system almost completely automates the paperwork associated with the daily trading of all types of credit instruments. After each transaction the company's portfolio is automatically updated, and necessary receipts and bills for delivered and received securities are printed. At the same time, the system performs calculations, makes ledger postings, and provides instantaneous summaries of company financial status and holdings for management review.

Developed with help from R. Shriver Associates of Parsippany, NJ, the custom system is built around a pair of 3000 Series II computers from Hewlett-Packard, 1501 Page Mill Rd, Palo Alto, CA 94304. Initially it includes 16 input/output terminals, but it has capacity to add 16 more at out-of-town branch offices. Over the next five years it is expected to handle a volume of about 3000 security transactions each day, which is within the operational control capabilities of the computers.

The dual computers were included in the system design to provide redundancy. According to Bent Rasmussen, system designer and project manager for the security trading firm, "when you're dealing with security trades that entail millions of dollars in each transaction, you're in bad trouble if you can't operate. For example, if securities aren't delivered to banks before they close at 3 pm, thousands of dollars can be lost in interest."

Of the two computers, one (A) is normally online while the other (B) remains inactive. Each computer has two 15M-byte disc memory storage units which contain a file of all daily transactions, an inventory file of 1500 different positions, a security master file of about 1500 issues, and a master file of about 7000 accounts.

As transactions are recorded on disc they are also recorded on a magnetic tape on the A system. If system A breaks down, the A tape transfers the transactions onto the disc of the B system. At the end of each day, the transaction file is cleared from disc to prepare it to handle the next day's transactions.

Although computer B immediately takes over when it is placed online, several minutes are required for the A tape's information to be read onto the B disc. Current updating of the system will result in simultaneous real-time updating of discs on both A and B units.

When transactions are entered by operators—filling in spaces on a form displayed on a CRT terminal—the computer system checks for missing data, validates the account, adds or removes the security to or from the inventory, and prints a receipt or billing ticket multipart form that also includes the description of the agency or corporation issuing the security. The ticket is printed out on a terminal printer and is used to receive a purchased security or to deliver a sold one.

At the end or at any point during the day, the system can produce a complete and detailed list of the security inventory. In addition, customer files are updated, all transactions are calculated online, customer confirmations are printed, a pending file is maintained, the "stock record" is maintained, and required operations and management reports are produced.

Circle 160 on Inquiry Card

DC&AS BRIEFS

Process Control System Provides Application Flexibility

Designed expressly for process control, Polstar™ features a 32k- to 64k-word minicomputer, flexible disc memory unit for loading software and storing operating data, versatile process-oriented programming language (POL*3), fill-in-the-forms application package (ICAP), and full color graphic displays. The system introduced by Taylor Instrument Co, 95 Ames St, Rochester, NY 14601 is said to combine flexibility with simplified operation.

POL*3 software was developed for batch processes as well as continuous control. The high level language uses familiar process control terms to define operating



Zero RPM. The Disk that doesn't Spin.

Megastore goes where a disk drive used to go.

More to the point, Megastore keeps going long after a disk drive quits. Without motors, bearings, heads or platters, there's nothing to wear out, burn out or crash. No moving parts.

Megastore is the astonishing new fixed-head disk memory replacement from Ampex that uses reliable cores instead of rotating media. In the long run it saves a lot of money.

Megastore provides increased throughput, increased system availability, increased system uptime and reduced maintenance costs. A vastly better return on investment.

Unplug your disk and plug in Megastore. You'll get a half-million to four million bytes of capacity (in half-megabyte increments) that your existing software can't tell from the disk it was designed for. The only difference you'll see is a major improvement in throughput, because Megastore has a data access time that's anywhere from 1000 to 3000 times faster than the disk it replaces.

Megastore. Ready now as a software-transparent replacement for Novadisk (Megastore 1223) and DEC's RJSO3/RJSO4 Disk (Megastore 11). Also available as Megastore 4666 for users who wish to provide their own controller. Other versions on the way. Contact Ampex Memory Products Division, 200 North Nash Street, El Segundo, California 90245. Phone (213) 640-0150. Ask for Megastore. The disk that doesn't spin.

AMPEX

Novadisk is a trademark of Data General Corp.

CIRCLE 31 ON INQUIRY CARD

DC&AS BRIEFS

procedures with a minimum of programming, and can be used for supervisory setpoint control, direct digital control, sequential control, and process optimization. Priority execution of control procedures allows any procedure to be assigned one of 31 different levels of priority to insure timely response to the wide range of parallel operations required to control complex processes.

ICAP is a set of prewritten subprograms that handle all the usual process control and communication functions without user programming. To apply the system to a particular process, the user lists specific process and control parameters on standard data base forms. This information is entered in the system via an operator-system dialogue. Without further programming, the system can provide I/O handling, control calculations, alarms, logs of selected data, and five different interactive displays of process and system status.

The system minicomputer features real-time clock, hardware multiply/divide, 64 priority interrupt levels, and automatic power failure/restart. Support peripheral devices include dedicated line printers, paper tape and card handling equipment, and black and white or full color CRT displays. A microprocessor-driven Colographic™ console features pushbutton-access to any display.

Controller Malfunctions Identified By Added Package

A hardware/software error detection and indication package (EDIP) that locates and identifies about 75%



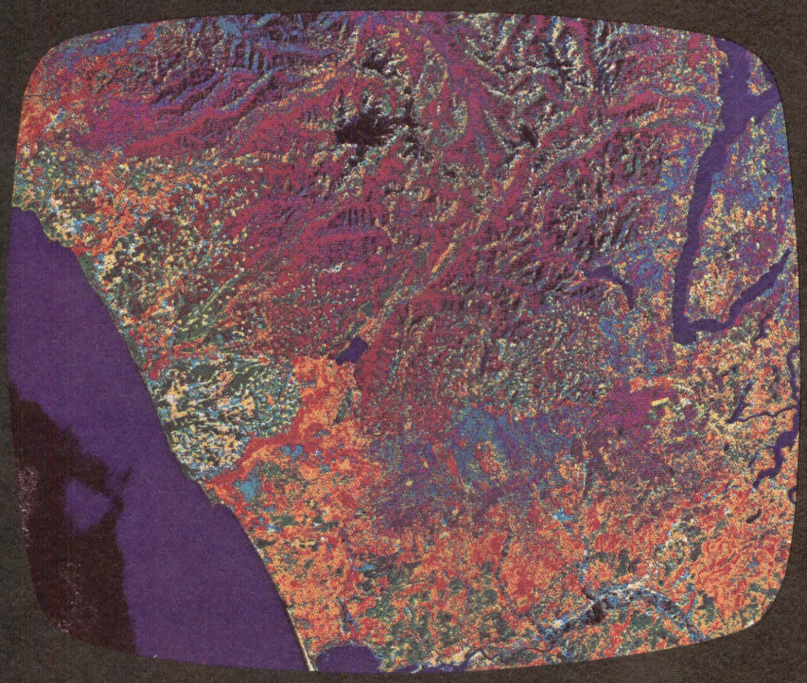
of potential or actual failures of the EPTAK™ microprocessor controller (*Computer Design*, Dec 1975, pp 35-41) has been introduced by the Eagle Signal Div of Gulf + Western Manufacturing Co, Davenport, IA 52803. (This eases identification of the remaining 25%.) Malfunctions that are either internal or external to the control system are brought to the operator's attention. The package, available with both new systems and those already installed, provides early warning of system degradation, immediate alarm in case of actual failures, indication of system self-correction when it occurs, and simplified software debugging and system installation.

Components of the package are factory-programmed software, operator's manual, and watchdog timer (WDT) and error indicator (EI) modules. The WDT module, which requires about 20 lines of user programming, consists of two independent software timers which provide visual and audible alarms when predesignated routines are not completed within preset time intervals. LED indicators on the face of the EI module identify the failure.

Centralized Control System Incorporates Interface System for Component Intercommunication

Process controllers are now linked through a communications processor with operator CRTs, operator trend terminal, system formatter, and optional host minicomputer by an ASCII 8000 centralized control system. Incorporating its ASCII 8000 computer interface system (*Computer Design*, Oct 1976, p 70), Beckman Instruments, Inc, Process Instruments Div, 2500 Harbor Blvd, Fullerton, CA 92634 designed the control system to ease bidirectional communications between remotely located controllers and a central control room. It is said to be practical for large, multiloop control applications or small systems where controllers are scattered throughout the plant.

The communications processor, which serves as a communications director and system controller to scan and address all of the peripherals and controllers in the



This display shows the Quinault Indian Reservation in Washington state. 16 separate colors have been assigned for such categories as Burn Areas, Forest, Brush and Bare Land.

Bendix Aerospace Systems Division uses a Ramtek display generator to really show its colors. The Bendix Multispectral Data Analysis System (M-DAS) provides a clear, color-coded display for analysis of data from NASA's LANDSAT. And by using Ramtek's moving window display—or scroll—they're able to look at more data at one time than can be displayed on the still screen. Images of the same areas may also be correlated so that changes between past and present can be referenced.

Bendix is but one of a growing number of customers who are finding that Ramtek's modular graphics and imagery systems are giving them the expandability, flexibility and increased productivity they need. Besides the basic alphanumeric and imaging capability, Ramtek offers a wide variety of other functions including graphics — vectors, conics, plots, bar charts — pseudo color and grey scale translation.

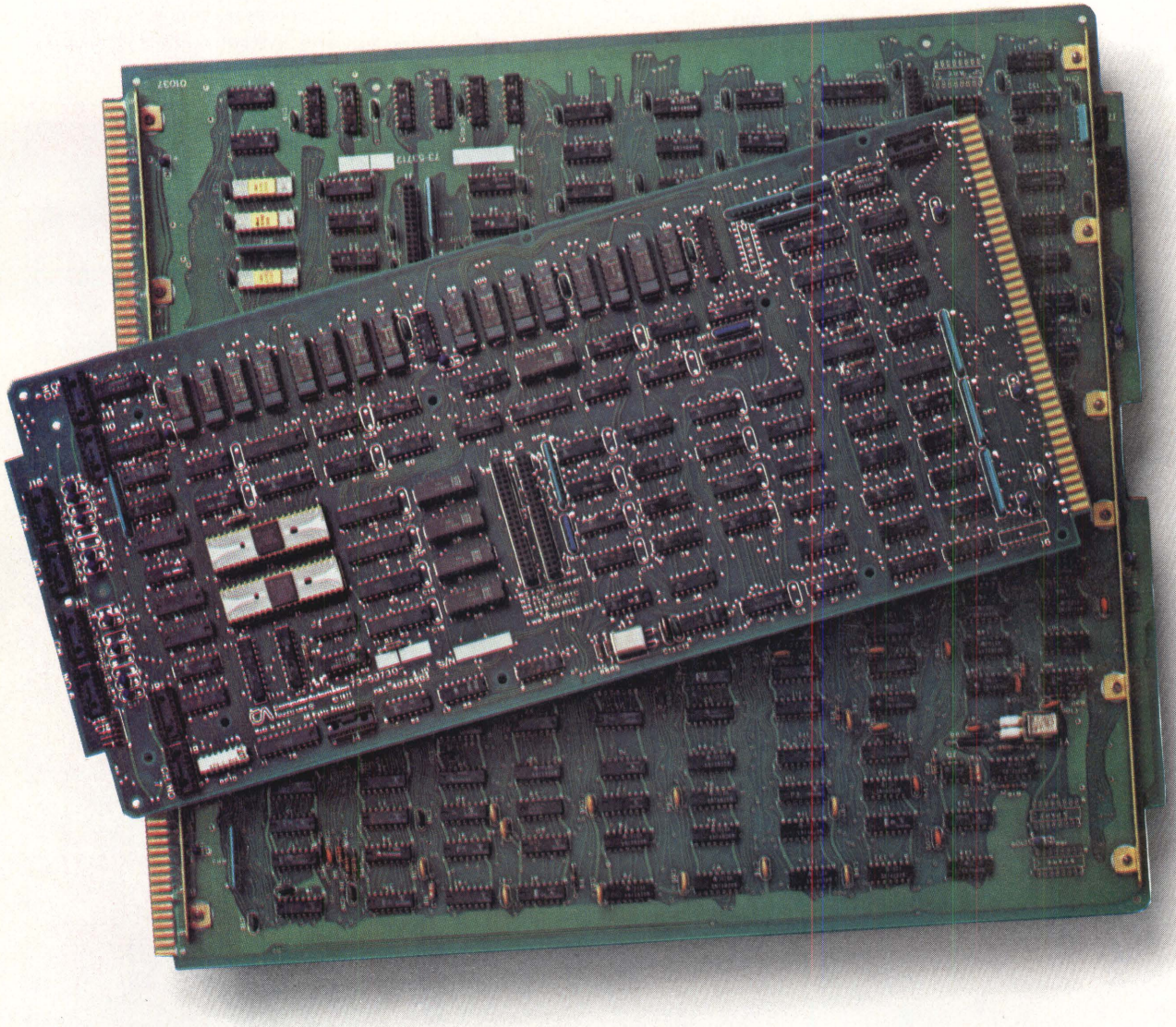
Because the Ramtek RM 9000 family is totally controlled by a standard 8080 microprocessor, it is easy to develop and download your own control software.

To find out more about how Ramtek can show off for you, call or write: Ramtek Corporation, 585 North Mary Avenue, Sunnyvale, California 94086; (408) 735-8400.

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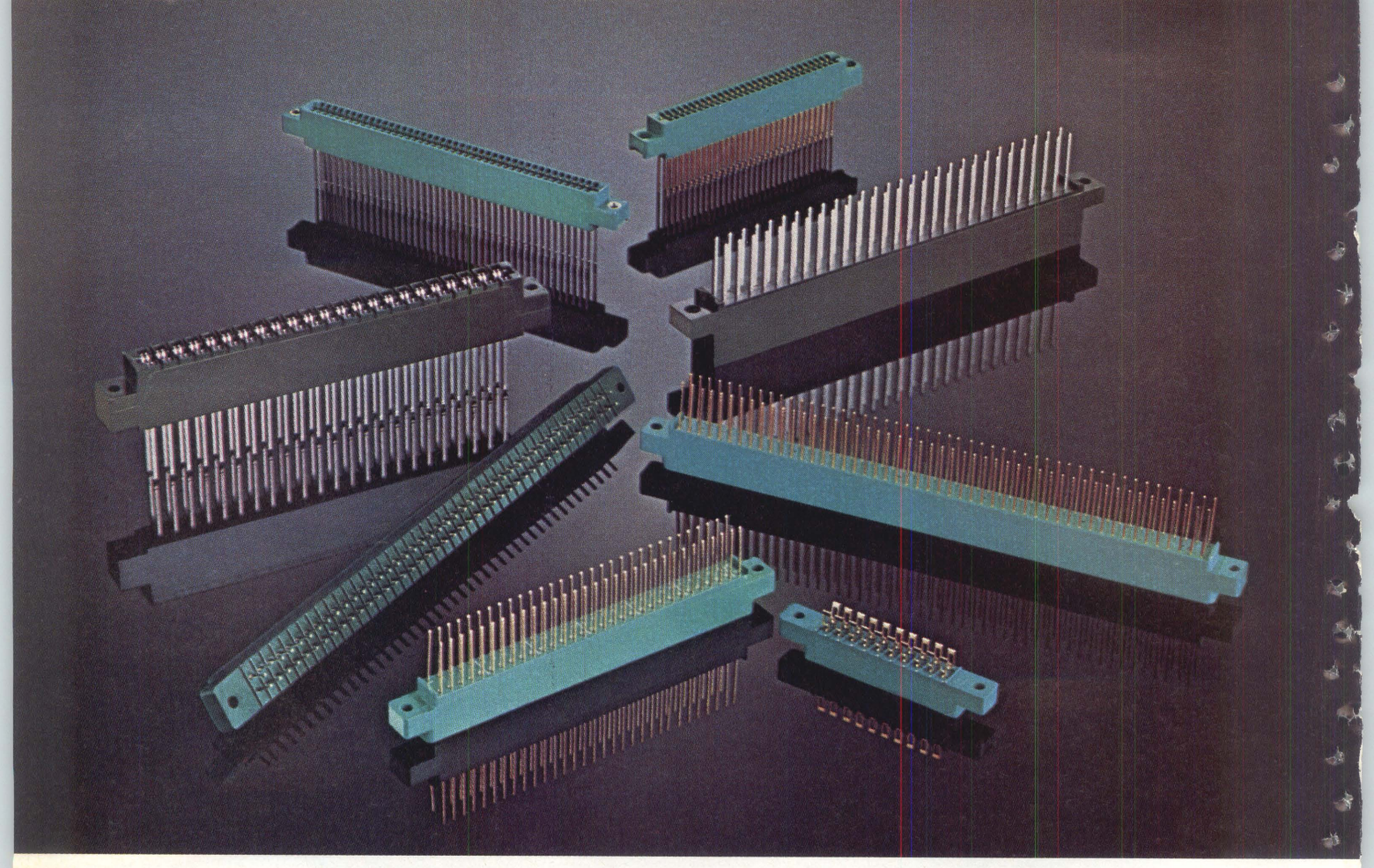
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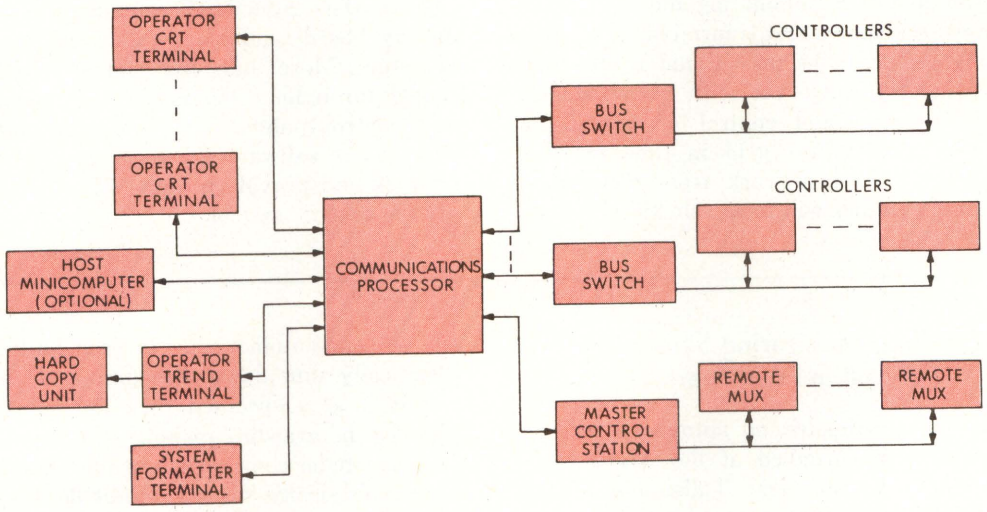
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DC&AS BRIEFS



Beckman centralized process control system. Communication processor serves as director and system controller, utilizing computer interface, to scan and address all peripherals and controllers

system, is expandable to 64k bytes of memory and 34 RS-232 interface ports. A software package provided with the system resolves timing differences between incoming and outgoing data, and contains alarms, calibration, and identification for the controllers. Processor hardware is totally redundant. Each circuit board is duplicated. A built-in fault detector automatically switches from a board to its backup board if a fault occurs. Switching between boards may also be performed by the operator. All communication within the system takes place in ASCII over asynchronous bit-serial data highways.

A system formatter terminal performs reconfiguring, labeling, tagging, and basic system layout functions. Cassettes allow any changes in the system's configuration from initial startup to be recorded on tape so that the plant can be restarted quickly after a shut down. An operator trend terminal with hardcopy unit is a microprocessor-based color graphics terminal, equipped with core storage for trending analog inputs at 10-min intervals for 24-h periods. Upon operator request, the terminal will display a graph of a particular variable, scaled in engineering units. If a hardcopy is needed, an associated printer is activated.

Intelligent operator CRT terminals, used to interrogate and command the processor, provide deviation, group, and loop displays which enable operators to view as many as 256 deviation displays at a single time. Data are presented in a series of 32 bar graphs, each with eight loops. A bar is normally green, but upon reaching an alarm point (set in the software program), the bar turns red. An additional software deviation alarm may be incorporated to cause the bar to flash red.

After determining which loops are in deviation alarm conditions, the operator can call up eight loops, showing all the parameters associated with the loops. An additional single loop display details operating parameters, deviation limit, and settings. While viewing these displays, the operator can issue commands to the controller via the display's keyboard.

Various levels of backup are provided. If a data highway fails, the plant remains under automatic control by the individual controllers that may be accessed directly or through a backup panel. If a host computer is in the system and fails, the system reverts to automatic control. Since each loop has a dedicated controller, a controller failure causes the loss of only one loop.

DC&AS BRIEFS

Energy Control System Incorporates Multiple Mainframe Computers

A $16-million computerized energy control system is being supplied by Control Data Canada, Ltd to Hydro-Quebec in the first phase of automating the provincial network for energy production and transmission. A provincial dispatching center, to be operational by the fall of 1979, will provide Hydro-Quebec with instantaneous acquisition of information and control of operations throughout the provincial power grid in time for the integration of power on the network from the James Bay power project. Operators will have reliable information on the entire network, be able to study computer models of the network, evaluate alternative operational techniques, and implement operational procedures.

The system, to be installed in Montreal, will include two Canadian-made CYBER 173 computer systems, four Control Data System 17 computers, a large operational display board, and color display screens for up to 35 operators. More than 135 remote terminals will be installed throughout the network to provide information and control points. The computer company also will develop the software necessary for the operation of the network and provide training of personnel on operation of the control system.

Energy Control/Monitoring System To Pay For Self in Four Years

According to Air Force estimates, an automated facility management system to be installed at the Arnold Engineering Development Center, near Tullahoma, Tenn, under a contract awarded to Hughes Aircraft Co's Microelectronic Products Div, 500 Superior Ave, Newport Beach, CA 92663, should reduce the Center's annual energy usage by $130,000 and labor costs by $94,500. The system will provide automatic control of a primary pumping station and will monitor and control most of the heating, ventilation, and air conditioning equipment in 42 buildings (presently controlled either manually or semi-automatically in each building). It will automatically shut down the equipment each evening and restart it at a specified time the next morning. There will also be growth capability for other, future services.

A computer-controlled central station will remotely access physically distant terminals via a single wide-brand coaxial cable and microwave link. Data will be transferred between remote terminals and the central station using time-division multiplexing at 1M bits/s.

Growth capability will be built into the system to permit other services to be added at a future time. For example, the coaxial cable will provide sufficient bandwidth to transmit closed-circuit television and voice in addition to the monitoring and control data.

Microprocessor Expands Capabilities of CNC System

Incorporation of a microprocessor in the CNC 2800 enables calculations to be carried out in 0.0001″ (0.0025-mm) increments at speeds up to the full capability of each machine tool. The standard microprocessor computer numerical control (CNC) unit—now in production by Posidata Ltd, Rankine Rd, Basingstoke, Hants RG24 OPP, England—contains software for inch/metric switching from tape instructions, automatic acceptance of EIA or ISO coded tapes, continuous path slope and arc operation, up to six axes of simultaneous linear moves in absolute or incremental programming, or a mixture of both; feed rate and spindle speed control from tape, mirror image operation from tape, programmable dwell, and cutter compensation. The last item consists of 32 pairs of tool length or tool diameter offsets which are keyboard entered at will.

Operation can be from tape with or without edit modifications, or, alternatively, the tape can be entered in the 5.5k-character memory. A tape punch output interface enables new tapes to be prepared from the old tape with appropriate modifications or direct from memory. A cutting operation can be halted in mid-cut, the tool jogged away from the work, and the tool subsequently returned precisely to the point at which the sequence was stopped. Repetitive machine operations can be performed by means of a cycle file memory which enables files to be "nested," ie, one repetitive sequence to be called up within another. Cycle files can be performed up to 99 times by means of a file multiplier.

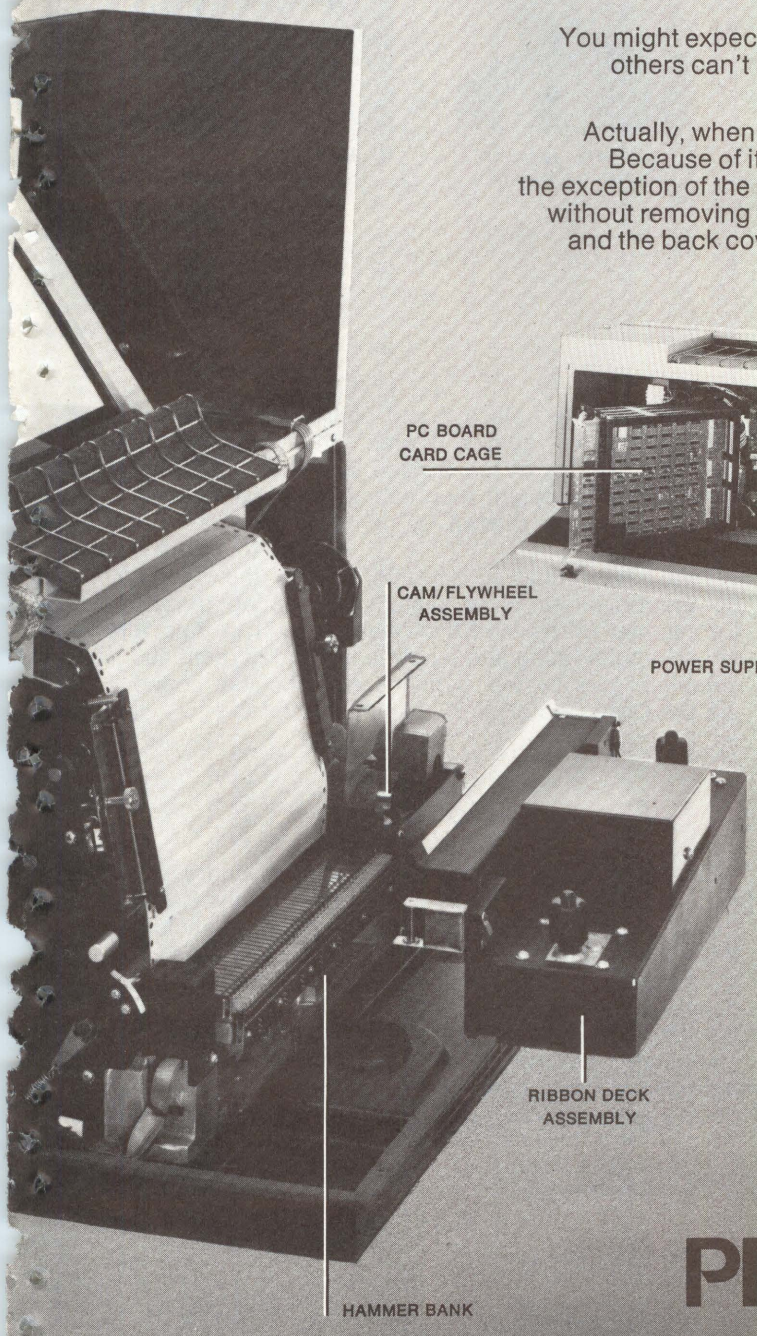
A CRT display provides information on the current program (current sequence and modal instructions) as well as absolute or incremental dimensions. It also can show all offsets, details of any editing which has been carried out, and self-diagnostic performance routines. Programming is eased by decimal point numbers with the plus sign omitted. Dimensions can be entered up to seven digits. All edited and offset memory information is retained up to 72 hours with power off. □

The concept and design of the Printronix 300 Impact Matrix Line Printer/Plotter offers you several remarkable cost/performance advantages.

Like dramatic savings in service costs from modular construction.

You might expect a precision 300 lpm line printer that produces print quality others can't match, and doubles as a plotter, to be a monster to service.

Actually, when compared to servicing other printers, it's easier and faster. Because of its modular design, the maximum MTTR is 30 minutes. With the exception of the main motor, all functional modules can be quickly removed without removing the shroud, as shown in the photos of the front cover raised and the back cover open. But that's only one reason why maintenance and service costs will be far lower than with other printers.



A Printronix 300 never requires character alignment or hammer flight time adjustment like other printers. Even the hammers and/or coils can be field replaced. And its mechanical simplicity extends MTBF so far that less servicing is required. That's why we've offered a one-year warranty from the beginning. Write for our brochure. You'll see why you'll have less downtime and fewer service calls. In short, a lower cost of ownership.

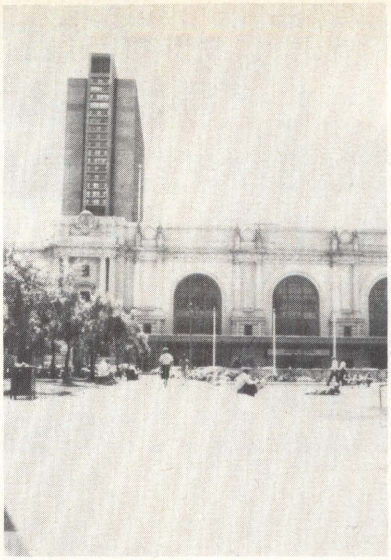
Printronix Inc., 17421 Derian Ave., Irvine, CA 92714. (714) 549-8272.



PRINTRONIX 300

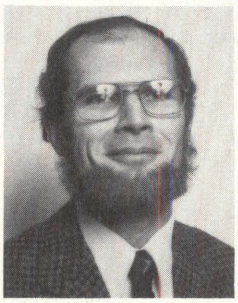
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CIRCLE 34 ON INQUIRY CARD



WESCON|77

September 19-21
San Francisco



L. Terry Jackson
Program Chairman



Dr Bernard M. Oliver
Keynote Speaker

"Electronics at the Golden Gate" sets the theme for the 26th annual Western Electronic Show and Convention in San Francisco—a key city in the western electronics marketplace—featuring a 3-day professional program which zeroes in on needs, trends, and applications of the technology in real terms and in real time. As a gateway to a strong, solid electronics market, WESCON/77 offers professionals and students alike a prime opportunity for a practical, technical update of important trends in technology. The 32 professional program sessions were organized by L. Terry Jackson (Lawrence Berkeley Labs), program chairman; Alan B. Grebene (Exar-Integrated Systems) is vice chairman.

Sponsored by the San Francisco Bay Area and Los Angeles Councils of IEEE, and the Northern and Southern California Chapters of the Electronic Representatives Association, the show features a 680-booth exhibit in conjunction with the sessions.

Special Activities

Two events—the Wescon Luncheon and the 23rd Wescon Distributor-Manufacturer-Representative (DMR) Conference—will preview the show on Sunday, Sept 18, at the St Francis Hotel. Delivering the keynote address at the luncheon will be Dr Bernard M. Oliver, vice president for research and development, Hewlett-Packard Co and past-president of IEEE. The DMR conference will be held during that afternoon at the St Francis.

Carrying over the conference's theme into two of the traditional social events, the all-industry reception on Monday evening at the St Francis will be "Fun and Games at the Golden Gate," featuring audience participation in the electronic and TV games which will be operating in the hotel's grand ballroom for the entertainment of the guests. Women-at-Wescon will take part in a "Cruise of the Golden Bay," first crossing to Tiburon for shopping, then sailing to Angel Island for a luncheon. Also offered is the Wescon Film Theater presentation.

Two bus systems in operation during the week will be the Bayshore Flyer system connecting the Civic Center, the Hilton, and the Cabana Hotel in Palo Alto on a regular schedule each day; and a continuous commuter bus system within San Francisco, connecting the Civic Center and downtown hotels.

Exhibits

With 400 exhibitors introducing products and systems in 680 booths, the exhibits will occupy Brooks Hall and the adjacent San Francisco Civic Auditorium, including the main auditorium and Polk and Larkin Halls. This showcase of products is expected to attract a large, qualified audience of working technologists to evaluate the display covering production, packaging, and test equipment; instruments; mini and microcomputers and peripherals; and components and micro electronics. Show hours are 9:30 am to 6 pm on Monday and Wednesday, and 9:30 am to 9 pm on Tuesday.

Registration

Computerized registration at the show will take place at the Civic Auditorium and San Francisco Hilton Hotel. The fee of $5 covers all exhibits and professional program sessions for the three days.

(*Continued on p 68*)



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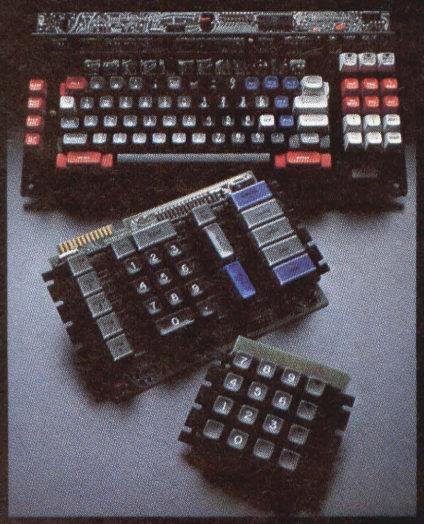
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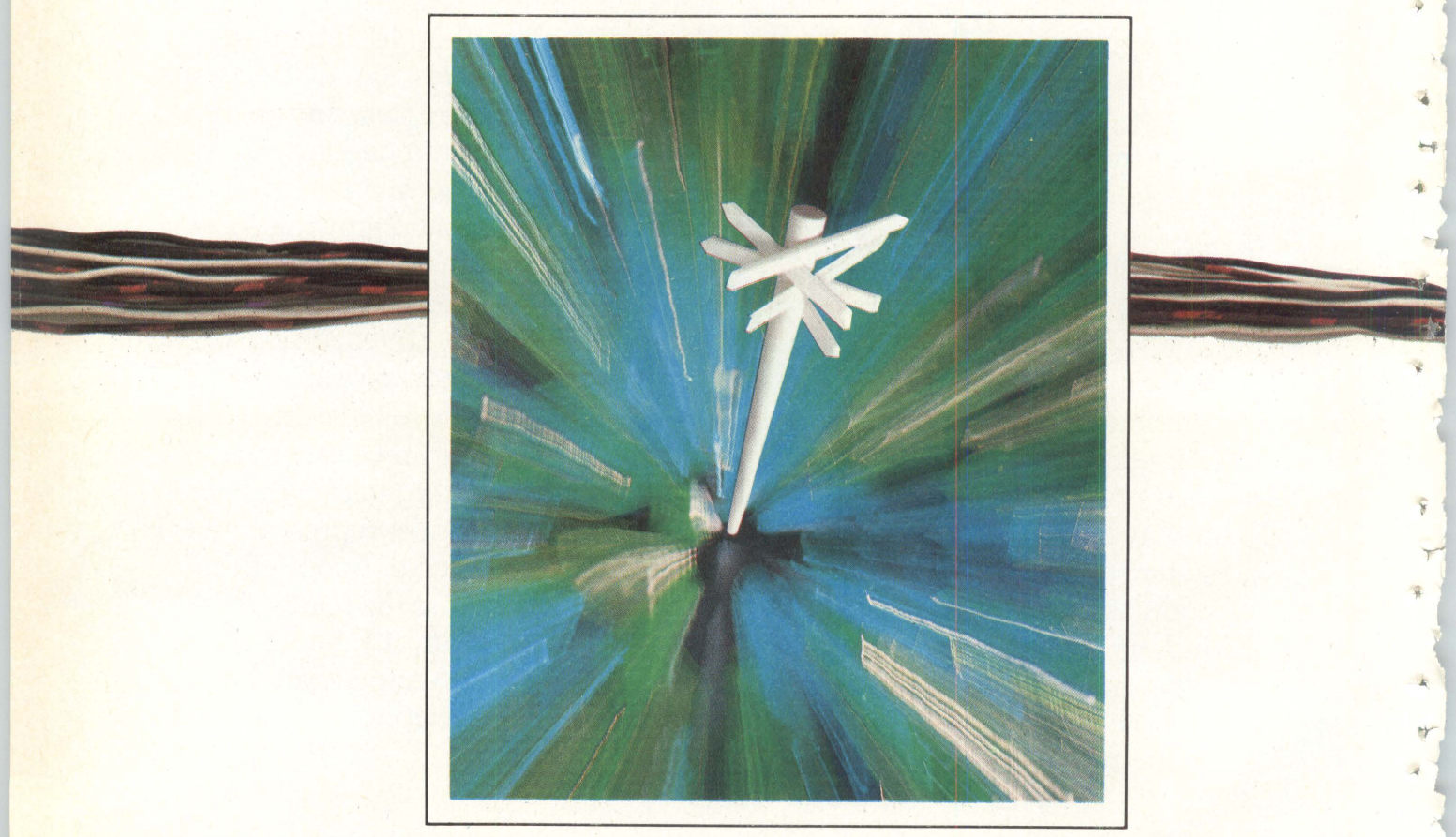


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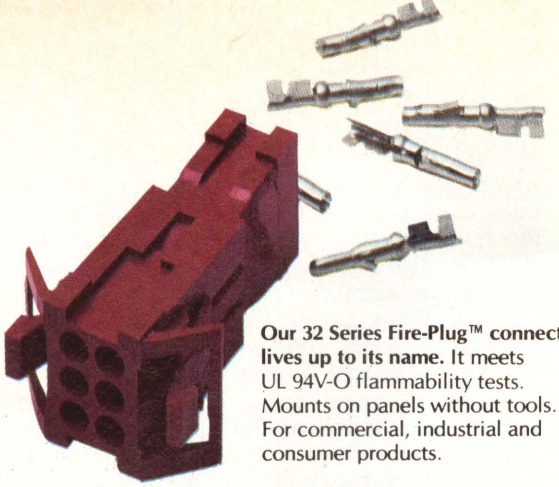
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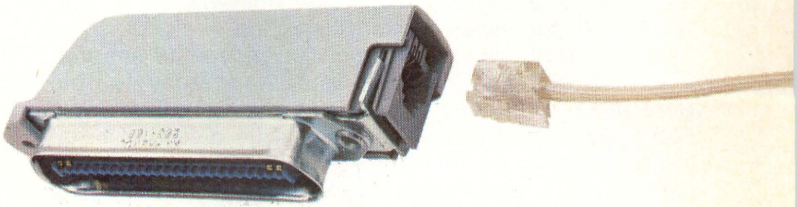
Our ideas. Your ideas. They're right for each other. To learn why, just call us at (312) 986-2320 or write to: Amphenol North America Division, Bunker Ramo Corporation, Dept. L-77, 900 Commerce Drive, Oak Brook, Illinois 60521.



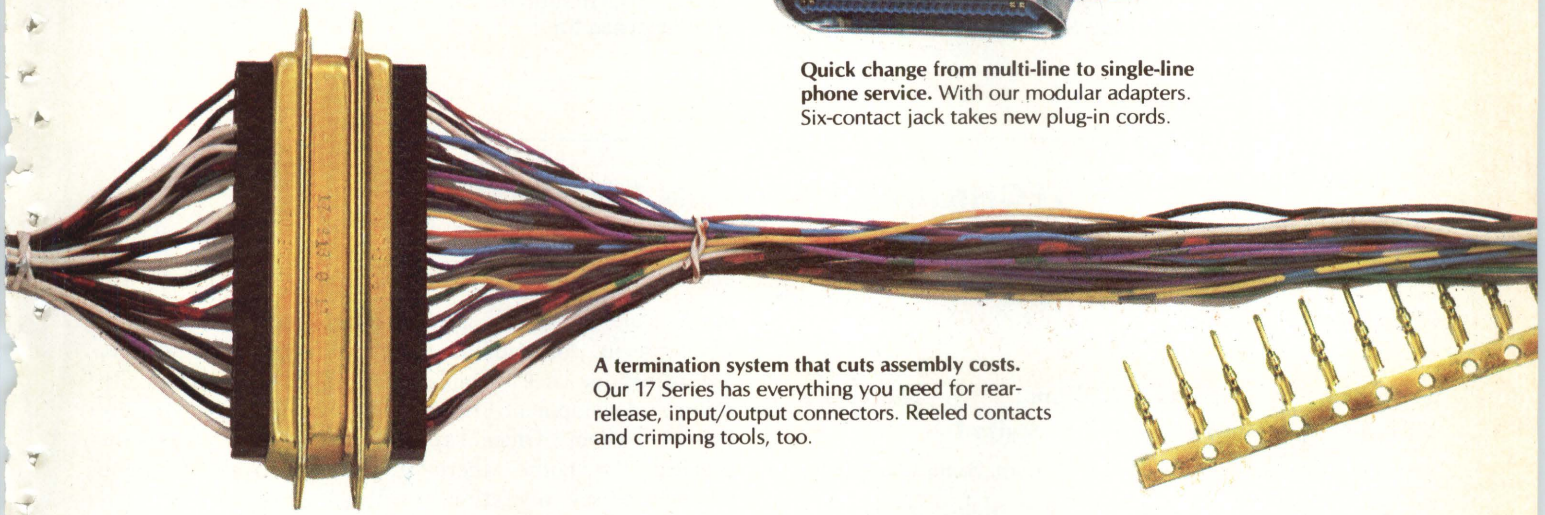
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CIRCLE 38 ON INQUIRY CARD

Professional Program

Confronting problems faced by designers and engineers in all aspects of their work, the sessions give an overview of applications, technology, advances, and future directions of the electronics field. Obtaining a balance of ideas from both manufacturer and user viewpoints, the 32 half-day sessions attempt to draw together all facets of a specific topic to enable attendees to acquire an awareness and clearer view of issues, and to provide them with answers or, at the very least, guidelines for further action.

Five sessions will be held concurrently at 10 am and 2 pm on Monday, Tuesday, and Wednesday in the Continental Ballroom complex of the San Francisco Hilton Hotel. Key to the program is its diversity, both in the way it is carried out—with panels, papers, and films—and in the subject matter covered. Major areas which are highlighted include microprocessors and other LSI peripheral circuits, automatic test equipment, IIL technology, distributed processing, time domain measurements, large scale computers, pocket calculators, semiconductor memory devices, switching power supplies, and IC testing.

Two sessions and a special exhibit have been planned as career aids to university-level engineering students. A panel session on Monday morning will cover engineering careers and problems encountered by those over 40; Monday afternoon's panel discusses the job interview. Both sessions are scheduled for the TowneHouse Hotel. A special exhibit of projects created by IEEE Region 6 student competitors will be on view at Civic Auditorium.

Only those sessions of particular interest to *Computer Design* readers are discussed in the following pages. Information is necessarily limited to that available at press time.

TECHNICAL PROGRAM EXCERPTS

Monday Morning

Session 2 — 10 am—12:30 pm — Continental Ballroom 5

New Advances in Peripheral Circuits I

Organizer/Chairman: Rob Walker, Intel Corp, Santa Clara, Calif

LSI peripheral circuits are now available which enhance performance of computer systems. Dedicated function controllers for microprocessors, SDLC protocol, CRT terminals, and A-D/D-A converters for floppy discs increase system performance and versatility. For larger systems, bipolar LSI high performance memory controllers and media encryption bit slices are available. The rationale behind the evolution of peripherals for microcomputers, various hardware/software tradeoffs, and the future direction of system architecture and performance are covered by Ken McKenzie, Intel Corp, while Barry Harvey, Siliconix, examines the use of ADC techniques for interfacing microcomputers. Andrew Allison, Advanced Micro Devices, individually outlines three advanced support circuits which eliminate microprocessor limitations in high performance applications. Bit-slice partitioning of the data encryption standard algorithm for use in both communicated and stored data is explored by Krishna Rallapalli, Fairchild.

Session 3 — 10 am—12:30 pm — Continental Ballroom 6

Program Development for Microprocessors: Emulation and Simulation

Organizer/Chairman: David Bursky, *Electronic Design* Magazine, Rochelle Park, NJ

ROM emulation tools, software simulation techniques, separate hardware and software development, and high end microcomputer development tools are various techniques employed to speed microprocessor program development. An emulator for the target ROM or p/ROM, according to Dick Woods, Data I/O, can drastically reduce development times. Michael Rooney of the Boston Systems Office explains that software has now reached the point where it can effectively simulate microprocessor operation, as long as capabilities and limitations are understood. Once the design is committed to hardware and firmware, the next step is system debugging, which Bruce Gladstone, Microkit, splits in order to handle hardware and software separately. While the microprocessor development system offers the most flexibility for system prototyping, Tom Clark, Tektronix, questions how much is really needed, highlighting features and cost/efficiency viewpoints.

Session 4 — 10 am—12:30 pm — Continental Parlor 7

Automatic Test Equipment for a Production Environment

Organizer/Chairman: Gerald Kutcher, Inforex Inc, Burlington, Mass

"Real world" problems experienced by manufacturing people are dealt with in this session which is structured for those who evaluate, purchase, and use ATE. Consideration is given to a conservative mathematical race detection technique needed to eliminate faults (Paul W. Accampo, Hewlett-Packard Co), requirements of microprocessor board testing (Noel P. Lyons, Fluke-Trendar), and LSI testing using parallel pin drive electronics (W. Nichols, Data Test). Selection of 4k RAM test patterns for go/no-go or characterization type test programs (W. Sohl, Macrodata Corp) and in-circuit inspection techniques for improved PC board assembly



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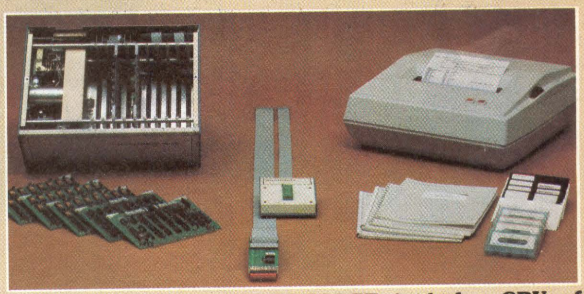
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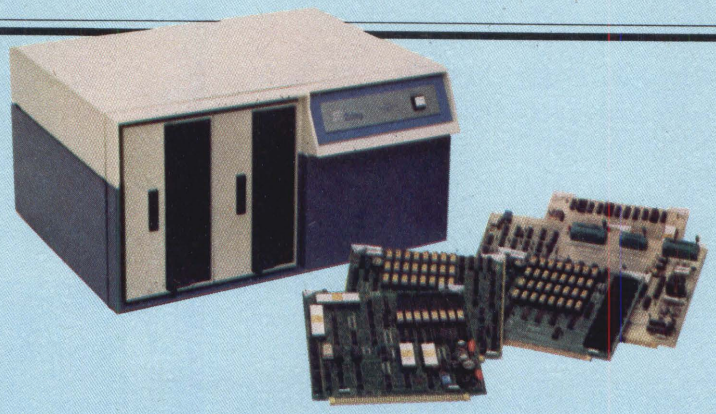
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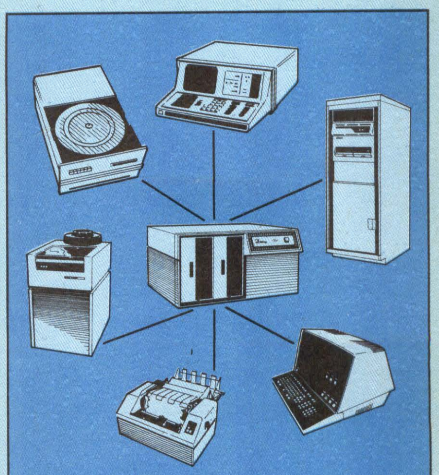
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process (R. N. Borrelli, Zehntel, Inc) round out the coverage.

Session S-1 10 am—12:30 pm Golden Gate Room

Engineering Careers and the Problems After 40

Organizer/Chairman: Harold Goldberg, Data Precision Corp, Wakefield, Mass

"This is my life professionally speaking. What kind of profession am I getting into? Is it a lifetime career or short-term job? What is this controversy about the 'over 40 engineer'? What can I do now to help me later?" are some of the doubts which possess the engineer. Prepared to help those involved in an engineering career to sort it all out is a panel comprised of Dr Albert Morris, Genesys Systems; Dr Robert Anderson, Purdue University; Dr James Rago, Jr, Cleveland State University; Dr James Mulligan, Jr, University of California, Irvine; and Huntz Cherney, IEEE.

Monday Afternoon

Session S-2 2—4:30 pm Golden Gate Room

Your Job Interview: The Million Dollar Decision

Organizer: Relations with Industry Group of the American Society for Engineering Education

Moderator: Ralph W. Keller, Stanford University, Stanford, Calif

The job interview is one of the most important career decisions, requiring proper preparation. This opportunity is afforded by a panel of professionals—Allen G. Borman, Rockwell International; George B. Coover, General Electric Co; Richard K. Daley, Bechtel Corp; and Harley A. Thronson, IBM—who direct recruiting of engineers. They will describe what their businesses are looking for, and offer suggestions on how to sell yourself.

Session 6 2—4:30 pm Continental Ballroom 4

Engineering Career Problems: Getting to the Bottom Line

Organizer: Jack Kinn, IEEE, Washington, DC

Chairman: John J. Guarrera, California State University, Northridge, Calif

Fundamental career problems, seldom examined in their full range and scope, must be dealt with in the context of current controversies in the profession. Engineers trained to deal with physical laws have greater difficulty dealing with social and political questions where there may be no true solutions—only informed choices. In the absence of cure-alls, the realities must be dealt with and some achievable alternatives to present negative conditions procured. Job security is of concern to Raymond Price, Stanford University, due to rapid technological change coupled with a slowdown in economic growth. John L. Lipp, Hay Associates, specifies what elements are considered and how they are weighted in determining compensation. Motivation and recognition are everchanging factors, as Donald B. Miller, IBM GSD, points out in exploring several concepts. Fundamental myths concerning management of engineers are dispelled as Dr Peter Graves, California State College, provides a fresh view of the ways the career environment may be nurtured, or in reality harmed by an organization.

Session 7 2—4:30 pm Continental Ballroom 5

New Advances in Microprocessor Peripheral Circuits II

Organizer/Chairman: Jim Vittera, Mostek, Carrollton, Tex

Many improvements in microcomputer system performance and cost-effectiveness are being made by the addition of sophisticated controllers to interface peripheral devices. The Z80 family of devices and the M6800 CRT controller are discussed by Ross Freeman, Zilog Inc, and Jack Kister, Motorola, Inc, respectively. Other topics include design and use of these devices and an overview of the past and future of microcomputer systems, with Adam Osborne, Osborne and Associates, identifying microprocessor characteristics which should have been present or were unnecessary in both the CPU and surrounding support logic. A panel composed of the speakers from session 2, in addition to Allan Oakes, NEC America, and Jerry Larson, Western Digital, discusses tradeoffs in using these devices.

Session 8 2—4:30 pm Continental Ballroom 6

Designing with Microprocessors: Difficulties and Dilemmas

Organizer/Chairman: Rudolph Panholzer, Naval Postgraduate School, Monterey, Calif

Coming to grips with some of the problems facing designers of microprocessor-based systems requires an awareness of various factors, which is supplied by Ken Rothmuller, Hewlett-Packard Co; Carol Anne Ogdin, *EDN*; Robert W. Ulrickson, Logical Services Inc; and Mona Saba, Tektronix Inc. Starting with the problem of proper selection of a microprocessor which is influenced by technical considerations and product development issues, the "language barrier" is then examined offering a review of languages and selection guidelines. A dominant problem is that of education and training; a manufacturer must be able to familiarize designers with microprocessors in the most efficient manner. A look at the pitfalls for the whole development cycle from inception to finished microprocessor-based products concludes the session.

Session 9 2—4:30 pm Continental Parlor 7

ATE Test Techniques for Complex Digital Assemblies

Organizer/Chairman: R. T. Szpila, GenRad, Concord, Mass

Thorough testing and fast, accurate fault diagnosis of digital PC boards is becoming increasingly more difficult with the advent of microprocessors and other LSI chips. State-of-the-art techniques are used to solve these problems. Both an ATE user and several manu-

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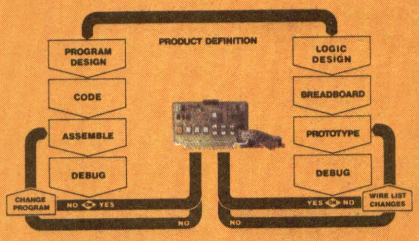
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facturers (Ed Steinberg, Digital Equipment Corp; Lutz P. Henckels, Instrumentation Engineering; Thomas S. Bush, GenRad, Inc; and Doug Cutsforth, Computer Automation) discuss present methods of testing microprocessor printed circuit boards, technical innovations in ATE hardware for testing CDAs, and software for test program generation.

Session 10 — 2—4:30 pm — Continental Parlor 1

Applications of Time Domain Measurement Systems

Organizer/Chairman: Norris S. Nahman, National Bureau of Standards, Boulder, Colo

Various computer-controlled time domain measurement systems are applied to the measurement of signals and networks in both the electrical and optical regions of the electromagnetic spectrum. Providing descriptions of these systems and their applications are Norris S. Nahman, NBS, discussing the Signal Waveform Metrology Program; Harry M. Cronson, Sperry Rand Research Center, explaining results of systems used to obtain properties of networks and materials over the 0.1- to 16-GHz frequency range; Fred J. Deadrick, Lawrence Livermore Laboratory, describing a time domain antenna range for scattering EM waves; and S. Gottfried, Bell Laboratories, commenting on properties of optoelectronic components.

Tuesday Morning

Session 11 — 10 am—12:30 pm — Imperial Ballroom

Designing With Integrated Injection Logic—IIL Comes of Age

Organizer/Chairman: Alan B. Grebene, Exar-Integrated Systems, Inc, Sunnyvale, Calif

IIL technology is seen from the points of view of both device modeling and LSI system design. Dealing with the modeling of IIL gates, Jim Smith, Tektronix, focuses on the relationships between IIL model parameters and process-related structural parameters, while D. B. Estreich and R. W. Dutton, Stanford University, describe problems and results of the development and use of a practical, user-oriented IIL macromodel. Covering specific LSI design approaches utilizing IIL technology are Keith Russell, Signetics, detailing the practical use of multilevel IIL in microprocessor design, and Louis Chan and Eugene Coussens, Exar-Integrated Systems, Inc, presenting an efficient approach to complex LSI design using mask-programmable gate arrays.

Session 12 — 10 am—12:30 pm — Continental Ballroom 5

Large Scale Computers

Organizer/Chairman: Harry G. Heard, Institute for Advanced Computation, Sunnyvale, Calif

This technical report to the industry updates the technology and applications of ILLIAC IV, covering developments in supercomputer and support memory system performance. Advance computer hardware and software applications are covered, with emphasis on large-scale optical memory data base subsystems. Theofanis Economidis, R. S. Lim, J. E. Korpi, Richard M. Brown, and Harry G. Heard, all of the Institute for Advanced Computation which operates and manages the ILLIAC IV (I4) computer system, comment on upgrading the system to operate in the 100-megaflop range. Also mentioned are interleaved codes for multiple-burst error correction for two laser memories, development of a software system for one of those memories, selection of optical over magnetic technology, and the role of central memory in a proposed I4 Tenex central system.

Session 13 — 10 am—12:30 pm — Continental Ballroom 6

Programmable Pocket Calculators: Onward and Upward

Organizer/Chairman: Rudolph Panholzer, Naval Postgraduate School, Monterey, Calif

While the development of more advanced, powerful calculators continues, the current generation of programmable pocket calculators offers incredible computing power and features such as nonvolatile memory, plug-in cartridges, and almost unlimited interfaceability. Updating the fast moving field of personal computing devices, Rex H. Shudde, Naval Postgraduate School, commences with an overview, Richard D. Cuthbert, Texas Instruments, continues with an outline of applications and anticipated growth, and James F. Chumbley, National Semiconductor, discusses factors involved with interfacing the hand-held calculator. Richard J. Nelson, Statek Corp, concludes the session with an explanation of users' clubs, which take up where manufacturers' applications support leaves off.

Tuesday Afternoon

Session 16 — 2—4:30 pm — Imperial Ballroom

Advances in Bipolar LSI Logic

Organizer/Chairman: Alan J. Weissberger, Signetics, Sunnyvale, Calif

Bipolar LSI logic elements, their potential applications, and design examples are introduced. The four devices are a family of programmable array logic devices aimed at replacing TTL SSI/MSI using bipolar fusable link technology (John Birkner, Monolithic Memories), the AM2903 microprocessor bit slice designed with a 3-port architecture (Bill Harmon, AMD), a field programmable logic sequencer which extends the domain of programmable logic to encompass Mealy state machines (Napolean Cavlan, Signetics), and a collection of high performance Schottky TTL microprogrammable building blocks (Rex Meek, Texas Instruments). A follow-up panel discussion explores trends and future directions in programmable logic.

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Session 17 — 2—4:30 pm — Continental Ballroom 5

New Generation Semiconductor Memory Devices

Organizer/Chairman: Derrell Coker, Mostek, Carrollton, Tex

New generation memory devices which exhibit performance and reliability characteristics far superior to previous devices are emerging onto the scene. Panelists, including Paul Schroeder, Mostek; Robert Frankenberg, Hewlett-Packard (both presenting papers); Bill Rigetz, Intel Corp; John Hewkin, Texas Instruments; Lin C. Wu, Amdahl Corp; and Gary Asbell, Datapoint, examine these products from both manufacturer and user viewpoints. Application problems associated with using these products, and problems of defining and designing products to meet user needs are also analyzed.

Session 18 — 2—4:30 pm — Continental Ballroom 6

Switching Power Supplies—Novel Circuits Approaches, Space Applications, and Characteristics Measurements

Organizer/Chairman: Abraham I. Pressman, Raytheon Co, Sudbury, Mass

Selection of the system block diagram of the switching regulator and its pulse width control scheme determines its reliability, cost, efficiency, size, and weight. Approaches described here offer simplicity and higher output powers, previously unattainable with conventional approaches. Neil Kepple, Keltec Co, covers the basic flyback switching regulator used in a high output power application, while Romualdas Dulskis and Joel Estey of Charles Stark Draper Laboratory, and Abraham Pressman, Raytheon, describe a unique magnetic-amplifier-controlled switching power supply; Derek Chambers and Dee Wang, Raytheon Co, concentrate on techniques for measuring parameters. Satellite radiation environment and airborne transmitter applications are described by Clement A. Berard, RCA Astro Electronics, and Robert Rosen, Hughes Aircraft, respectively.

Session 20 — 2—4:30 pm — Continental Parlor 1

The Use of Bit-Slice Microprocessors in High Performance Digital Signal Processing Systems

Organizer/Chairman: Howard I. Cohen, GTE Sylvania, Needham Heights, Mass

An examination of software, hardware, and application problems in realizing very high performance digital filtering and signal processing systems built with bit-slice microprocessors begins with a review and update of state-of-the-art technology. Methods of overcoming these problems, and design and application examples are supplied. Discussions offer information on software support problems, hardware organization to alleviate many of the software problems, applications in radar signal processing, and organizations to enhance digital filtering in radio astronomy and digital speech processing. Speakers, representing industry, government, and an academic institution, are P. C. Barr, Raytheon; M. S. Gerhardt, Digital Equipment Corp; J. Ardini, H. Cohen, and L. Sletzinger, GTE Sylvania Inc; Allen Peterson, Stanford University Center for Radio Astronomy; J. Clary, Research Triangle Institute; and L. Owens, Redstone Arsenal.

Wednesday Morning

Session 21 — 10 am—12:30 pm — Imperial Ballroom

Analog Interface in Microprocessor Systems

Organizer/Chairman: Narpat Bhandari, Signetics, Inc, Sunnyvale, Calif

Along with the advent of the microprocessor, monolithic bus-compatible analog products, such as A-D, D-A drivers, and other peripheral devices are assuming a key role in the realization of data acquisition systems. The papers survey ADC techniques and look at practical applications involving A-D/microprocessor interfaces (David Fullegar, Intersil); a 6-channel 8-bit microprocessor-compatible ADC (Russell J. Apfel and John Conover, Fairchild Camera and Instrument Corp); a microprocessor bus-compatible 8-bit system DAC (J. Simmons, Signetics); optimal D-A/A-D conversion techniques using a microprocessor (David Chung, Umtech Inc); and use of CMOS logic elements, microprocessors, and data converters in low power data acquisition WISE systems, suitable for field applications requiring independence from commercial power sources (Robert Pleva, Lawrence Livermore Laboratory).

Session 23 — 10 am—12:30 pm — Continental Ballroom 6

Transition to Distributed Processing

Organizer/Chairman: Jacob Sternberg, Conversational Systems Corp, New York, NY

Distributed processing is the logical conclusion to an evolutionary process. The elements involved in the past and current transitions are covered, followed by an examination of the impact of DP from three viewpoints. Jacob Sternberg and Jeffrey Goldfarb, Conversational Systems; Patrick LaMalva, Citibank; Tom Harris, IBM; and Mark Levi, National Semiconductor, comment on the management view (business reasons for embarking on decentralization), the technical planning view (technological reasons for distribution of processing resources, and analysis of technical problems), and the implementation view (the practical, orderly route of implementing the DP environment).

Session 24 — 10 am—12:30 pm — Pacific Room

Microprocessors: Communicating With the Real World

Organizer/Chairman: Andy Santoni, *Electronic Design* Magazine, Rochelle Park, NJ

As microprocessors find new applications and become less expensive, the complexity and cost of support circuitry become larger factors in system design. Larry A. Solomon and D. R. Carley, RCA Solid-State Div, explore software/hardware tradeoffs that can be made at system design to maximize processor utilization, and to decide whether software or a peripheral controller circuit is best for the job. Accessing peripherals from the microprocessor—as memory locations or via I/O ports—is addressed by Mitchell Gooze, Motorola Semiconductor Products. Dave Kress examines applying converters in microprocessor-based systems; and Mark Mayes and R. Wade Williams, GenRad Test Systems Div, explore methods of effectively testing complex peripheral chips to cut costs.

Wednesday Afternoon

Session 26 2—4:30 pm Imperial Ballroom

Analog and Digital Data Acquisition and Distribution with Microprocessors

Organizer/Chairman: Robert Morrison, Burr-Brown Research Corp, Tucson, Ariz

As microprocessors become more involved in real world applications, the ever increasing question is How is the interfacing performed? Numerous ways of performing the analog and digital interface function, as well as methods for handling digital problems such as contact closure sensing, are presented. Robert Morrison, Burr-Brown, gives an overview of the techniques and components. Preprocessing functions are examined by Claude A. Wiatrowski, U of Colorado, illustrated as frontend processing for industrial microcomputer systems. George Bryant, Datel Systems, details applications of analog conversion products in microcomputer systems. A specific application is described by M. L. Roginski and J. A. Tabb, Lockheed-Georgia Co, with the microprocessor-controlled fatigue load control system. Ivor Wold, Analog Devices, covers ADC and DAC integration in microprocessor systems.

Session 27 2—4:30 pm Hilton Plaza Room

Single-Chip Microcomputers Find More Than a Niche

Organizer/Chairman: Dan Hammond, Mostek, Carrollton, Tex

Trends in microprocessor applications including logic replacement, controller, automotive, appliance, and consumer products in the lowend logic replacement market are analyzed. A user's viewpoint and evaluation of available devices by Matt Biewer, Pro-Log, is coupled with discussions of three specific applications. Larry Goss, Intel, reports on the 8048-based keyboard/display module; John D. Bryant, Texas Instruments, discusses the TMS9940 microcomputer compared to the TMS8080A microprocessor used in a data terminal; and Mike Miller, Mostek, describes the implementation of an asynchronous serial data link using the 3870 single-chip microcomputer. A panel composed of these speakers and Marshall Kidd, General Electric, concludes with a discussion of some of the controversial aspects of single-chip microcomputers.

Session 28 2—4:30 pm Continental Ballroom 6

"ICs in Testingland"

Organizer/Chairman: Martin Marshall, *EDN* Magazine, Campbell, Calif

As a tale of semiconductor measurement techniques, "ICs in Testingland" expounds upon the necessity of IC testing, reveals the intricate mechanisms involved in memory testing, and adjudicates the microprocessor issue. The fantasy film is written and directed by Martin Marshall, *EDN* magazine, based on the format of "Alice in Wonderland." Following the showing of the original film, a panel comprised of Jim Fisher, Tektronix, Inc; Bob Huston, Fairchild Systems Technology; Bill Blatchley, Siemens Corp; and Floyd Kinnay, Continental Testing Labs, furnishes a discussion and question-and-answer period. □

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CIRCLE 46 ON INQUIRY CARD

IEEE Computer Society International Conference

Mayflower Hotel, Washington, DC
September 6-9

Concentrating on the theme of "Micros, Minis, and Maxis—Technology Thrust vs User Requirement," IEEE Computer Society's 15th International Conference will feature 28 technical sessions covering hardware, software, peripherals, technology, and applications. Under the direction of General Chairman, Paul L. Hazan, Applied Physics Laboratories, Johns Hopkins University, and Technical Program Chairman, Paul S. Skartvedt, TRW Energy Systems Division, COMPCON 77 Fall will touch on design, memory technology, and distributed processing. Evening sessions including a "hands-on" personal computing workshop are planned.

On Tuesday, September 6, preceding the Conference, three tutorials chaired by Victor R. Basili, University of Maryland will explore the practical and theoretical aspects of the topics discussed. Covering a broad spectrum of microprocessor technology and applications, "The Design and Application of Microprocessor Systems" will be highlighted by a "hands-on" workshop. "Distributed Processing" will address technological and managerial considerations in the design and applications of distributed processing.

Keynote sessions will commence at 11 am on Wednesday, September 7 with a presentation by Isaac Auerbach, president, Auerbach Publications who will reinforce the Conference theme with his "Forecast of Computer Technology, 1977-1985." Other keynote sessions will be held at 11, 11:30, 12 noon, and 12:30 to outline subsequent technical sessions. Eugene McFarland, assistant vice president, MOS Division, Texas Instruments, will keynote the *Microprocessor*-related sessions with "Microprocessors; Their Impact on Design Engineering." "Application Trends and Directions," presented by Joe M. Henson, vice president, Market Planning, Data Processing Div, IBM, will focus on *Computer Applications*. Tom Klein, National Semiconductor, will lead off the *Component Technology and Memories* area with "Trends in Future Memory Development." Delivering an "Overview of Distributed Processing" will be E. Douglas Jensen, Honeywell Systems & Research Center. "Peripherals in the Future" will introduce the sessions pertaining to *Peripherals*. Posing the questions, "Can Software Be More Like Hardware? Should It Be?" Walter Beam, U.S. Air Force, Office of the Assistant Secretary, Deputy for Advanced Technology, will initiate discussions relating to *Software*. Edson De Castro, president, Data General Corp, will launch the *Systems Technology* area with "Trends in Computer System Technology and Architecture."

Encompassing both hardware and software considerations, the *Microprocessor* section includes a session devoted to high level languages; more specifically, the correlation between language and usage. Offering suggestions for microprocessor software development and a proposal of a universal microprocessor systems software, "Microcomputer Development Techniques" deals with the developmental problems related to integration of hardware and software. Details on synchronous communications using LSI peripherals, vehicle control, and bit-slice microcomputing are offered in the session devoted to "Microprocessor-Based Controllers." "Systems Engineering with Micros" includes papers which evaluate various components of engineering such as queue memories, and avionics application.

Application trends and directions are explored in relation to medical, military, and real-time applications. The technological requirements and architectural considerations of signal processing are also noted. Real-time applications offered for consideration include papers on emulation considerations for real-time computer systems, and space-related control systems.

The *Component Technology and Memories* area focuses on specifics of such memories as bubble memories, CCDs, and RAMs, reveals the status of semiconductor memories in Japan, and indicates the direction of logic technology. A comparative evaluation of static vs dynamic memories can be found in "Memory Systems" which outlines a pseudo-RAM system with CCD-SR and MOS RAM on a chip. Advantages of CCD systems in future machine architecture and the usage of memory components are also discussed.

Various aspects of *Distributed Processing* such as hierarchical configurations, networks, and models are analyzed. Papers dealing with models and simulation present the results of a GPSS simulation of the AFOS closed loop store-and-forward communications network, and describe parallel control systems. Acknowledge Ethernet, and the Kent Distributed Control Project are two of the networks detailed.

Advanced and smart peripherals, state-of-the-art storage technology, and devices dominate the *Peripheral*-related sessions. Details of the design and simulation of a CCD-based display memory system for a microcomputer-controlled CRT terminal are examined.

Of interest to designers and systems engineers, the *Software* area includes a session on software engineering and development for microprocessors which concentrates on high level language programming, specifically to produce load modules for ROM in medium quantities. "Software Engineering and Development for Distributed Processing Systems" pinpoints the need for improvements in real-time distributed control software, and explores the means by which they are accomplished.

The approach to *System Technology* is in relation to past, present, and future. "Array and Directed Applications" discusses the Array 2 processor, presents a pipelined architecture bit-slice computer for high level languages, and tells of the evolution of parallel processor architecture for image processing. Implementation techniques centering on next generation systems include DBS architecture, design tools, and the use of multilevel encoding in microinstruction formats. An overview of trends in systems architecture is presented in "Mini and Multi Processors." □

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DR-121	1K x 10 2K x 8 2K x 10	900/350 ns 900/350 ns 900/350 ns	11.7" x 11.5" (297 mm x 292 mm)	+5V, −12V	25 Watts	Cambridge Memories' 1K x 9 Unicore
DR-104	4K x 9 8K x 9 16K x 9 32K x 9	750/350 ns 750/350 ns 750/300 ns 800/300 ns	13.5" x 8.3" (343 mm x 211 mm)	+5V, −12V	32 Watts	National Semiconductors' MOSRAM 104

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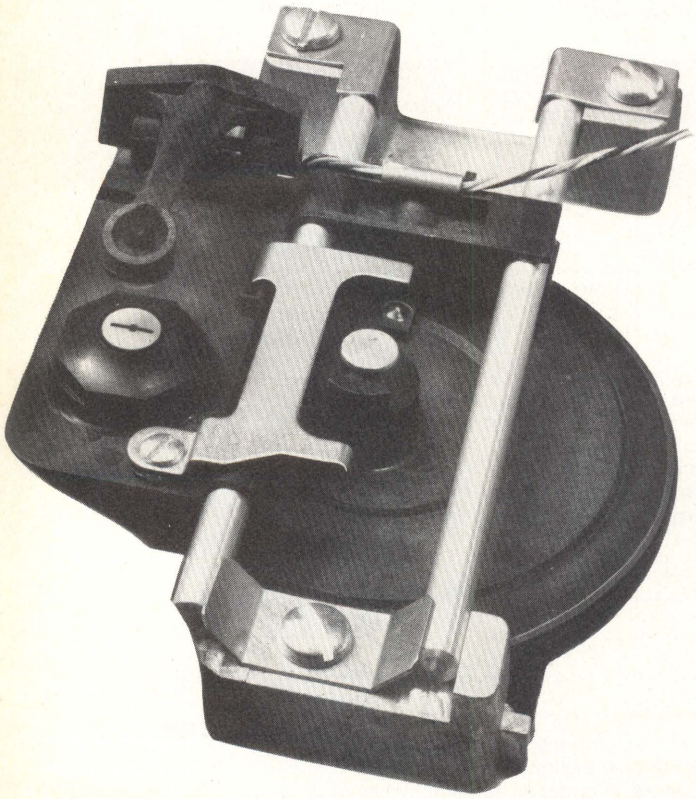
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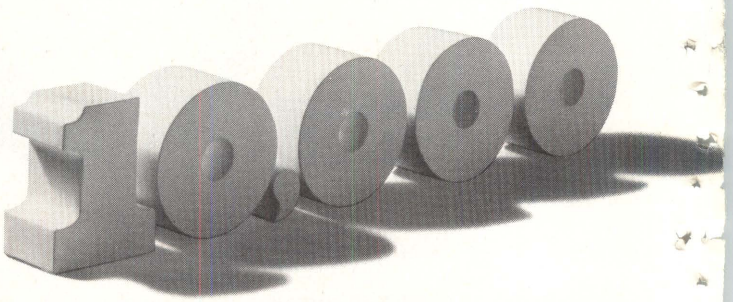
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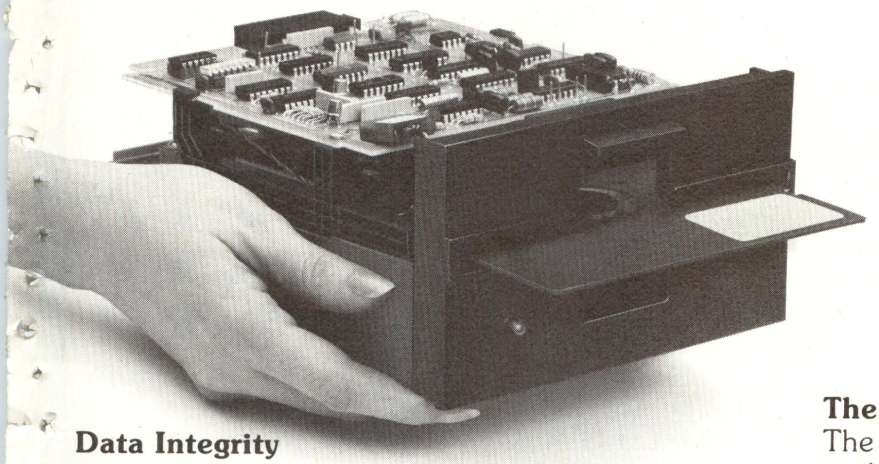
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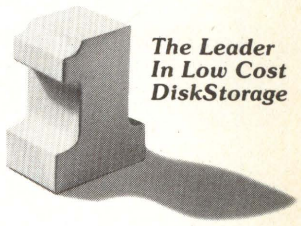
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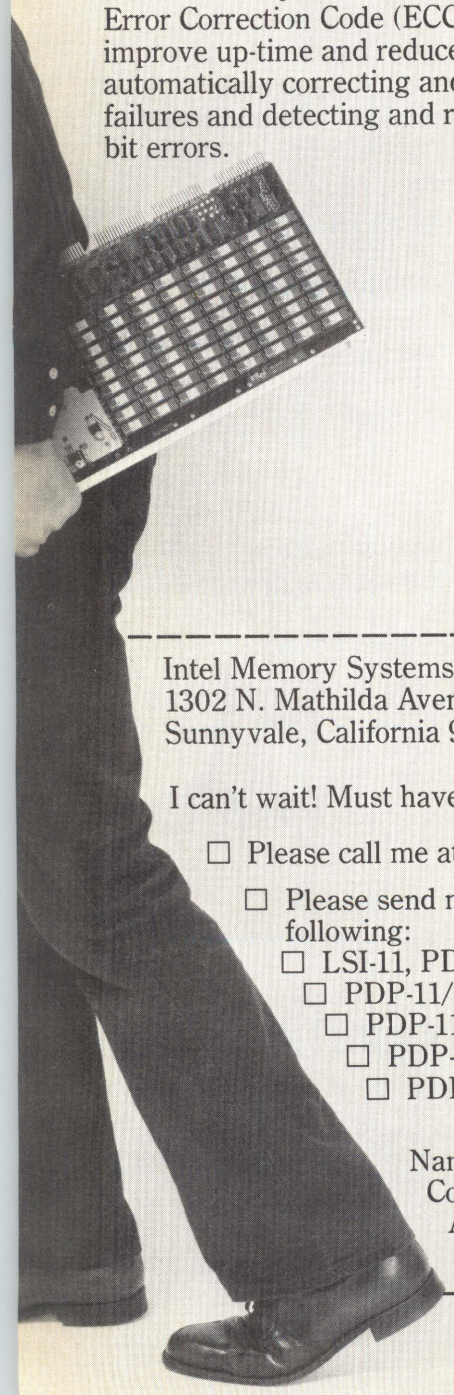
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CIRCLE 49 ON INQUIRY CARD

Tradeoff goals of a mid-range minicomputer design—balancing cost, functionality, and size for broad appeal—are primarily achieved by exploiting technological advances and appraising user needs

Design Decisions Achieve Price/ Performance Balance in Mid-Range Minicomputers

J. Craig Mudge

Digital Equipment Corporation
Maynard, Massachusetts

Design evolution of a minicomputer family usually proceeds along three basic dimensions: cost, functionality, and size. That is, the minicomputer becomes cheaper, more powerful, and smaller with time. The underlying hardware technology is the dominant factor in determining the evolution. In contrast to the evolution of large computers, market factors have less influence on the growth pattern of minicomputers. However, minicomputer software characteristics are affected by the market. These requirements rapidly feed down to modify the hardware, given that the technology will support user needs.

The DEC PDP-11/60* serves to demonstrate minicomputer designing with improved technologies. Being a mid-range machine, ie, neither the lowest in cost nor the highest in performance, its design is a rich source of tradeoff examples. Its cache design illustrates a price/performance trade, the decreasing cost of read-only memories (ROMs) show how hardware-microcode tradeoffs change over time, and its integral floating-point arithmetic unit exemplifies a software-hardware tradeoff.

Design Styles

Equipment history reveals that a member is added to a minicomputer family whenever technology advances by a factor of two; for example, doubling of bit density on a memory chip. Over the past 15 years, such an improvement has occurred about every two years.

These advances in technology can be translated into either of two fundamentally different design styles. One provides essentially constant functionality at a minimal price (which decreases over time); the second keeps cost constant and increases functionality. (Here, and in the discussion to follow, the definition of functionality has been broadened from its conventional single component, speed, to include components such as extended instructions and self-checking.) Both design approaches coordinate with the basic marketing philosophy of the minicomputer industry: more computation for more users at less cost. There have been ten models, or implementations, of the PDP-11 architecture since the unit was introduced in 1970.[1] Fig 1 illustrates how the two design styles affected successive implementations within this minicomputer family.

Lower cost members trace the decreasing-cost, constant-functionality curve. (This is the 11/20, 11/05, and LSI-11 or 11/03 line.) The horizontal line in Fig 1 connects the constant-cost, increasing-functionality designs. (Not shown are "growth-path" members that provide greater performance at slightly increased costs; 11/45, 11/55, and 11/70 machines trace an upward

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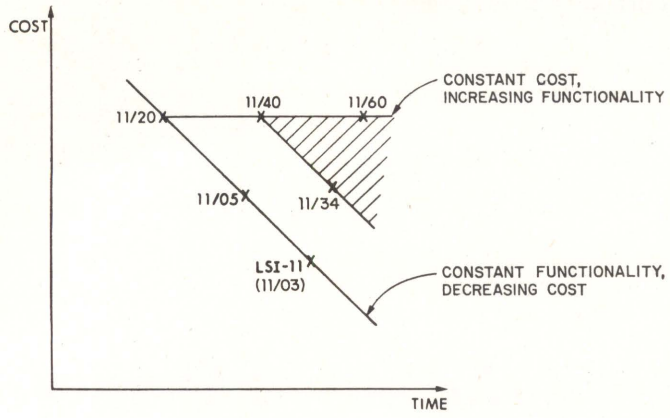


Fig 1 Minicomputer family evolution. Advances in technology translate into two design styles: constant-cost, increasing-functionality and constant-functionality, decreasing-cost. The 11/60 represents former design style. Functionality added to 11/40 is depicted by shaded area. Tradeoffs discussed occur within this area

growth-path curve.) Shaded area in the figure represents the added functionality possible through technology advances. Mid-range minicomputers attempt to optimize price/functionality and, hence, offer an excellent vantage point for discussing design tradeoffs made under the constant-cost design style.

In addition to the capabilities provided by technological advances, a mature family architecture and user base allows the minicomputer designer to include those capabilities that were not considered feasible in the original architecture. These features may not have been included because they were too costly to implement, not sufficiently general-purpose to justify their inclusion, or not perceived as being essential to users. Reliability, maintainability, the integral floating-point unit, and the writable control store (WCS) option represent such capabilities.

Internal structure of the 11/60 (Fig 2) incorporates a 2048-byte cache, memory management unit (for virtual-to-physical address translation), and an integral floating-point unit as standard components. The unit can perform a register-to-register add instruction in an average time of 530 ns; internal cycle time is 170 ns. Available as options are a floating-point processor, which implements at higher speed the same 46 instructions as the integral unit, a writable control store, and a microdiagnostic unit.

Advances in Memory Technology

Improvements in memory technology have been the principal forces in minicomputer developments. Memory

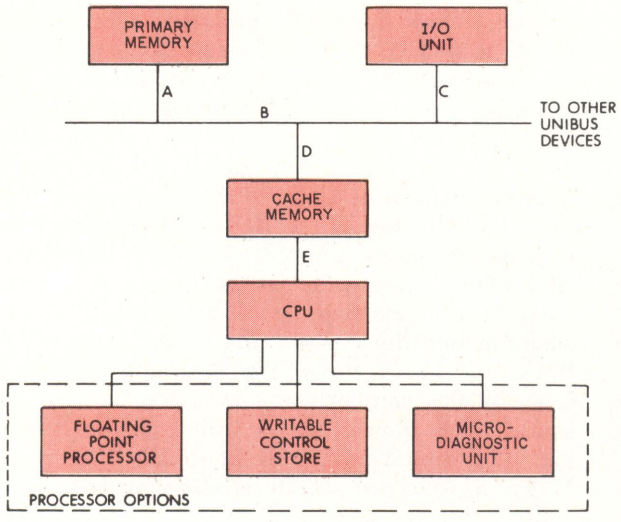


Fig 2 Internal structure. Cache placement between Unibus and CPU permits faster execution and allows use of standard memories. However, DMA monitoring mechanism is needed for traffic on path CBA. Module count is six for CPU and cache, one for writable control store, one for microdiagnostics unit, and four for floating-point processor. This processor operates in parallel with CPU execution of nonfloating-point instructions; instruction times are 1.02 μs for double-precision add and 1.53 μs for single-precision multiply. Writable control store uses 1024 control words that are reloadable and that control 170-ns inner machine. Machine is design optimized for user environment characterized by real-time operating system and FORTRAN

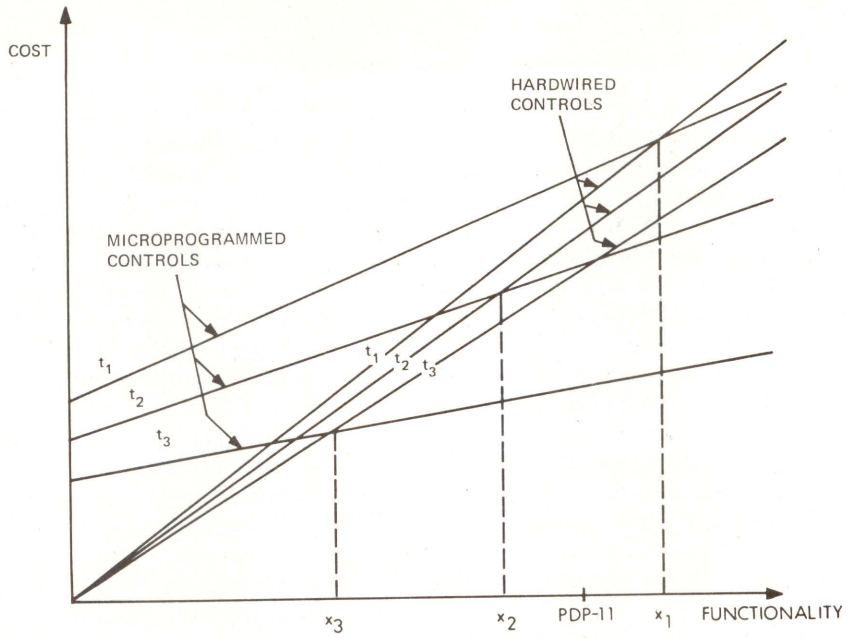


Fig 3 Semiconductor technology trends in control implementations. Cost comparisons, at three different points in time, of conventional hardwired control and advanced microprogrammed control show two important trends. First, at fixed point in time in 1970s (eg, time t3), microprogrammed control is less expensive above certain level of complexity (x3). For simplest type of machine, random logic gives most economical design. Microprogrammed design has base cost associated with address sequencing and memory selection circuitry. Microprogrammed control cost increases slowly with number of sequencing cycles, which are added as complexity increases, because each additional cycle requires one additional word of control store. Second, because rate of cost-decrease for memories is greater than the rate for random logic, cross-over points move with time, gradually shifting in favor of microprogrammed control. When 11/20 was designed (time t1) hardwired controls were cheaper. Its successor, the 11/40, was designed at time t2 and used microprogramming. The 11/60, at time t3, used increased microprogramming

is the most basic component of a computer and it is utilized throughout the design. In addition to obvious uses as main program and data memory, and as file storage devices (discs and tapes), memory is also located within the central processor in the form of registers, state indicators, control, and buffer storage between the central processor and main (primary) memory. In input/output (I/O) devices, there are buffers and staging areas. Memory can be substituted for nearly all logic by substituting table lookup for computation.

The constantly increasing bit density mentioned previously has been the most dramatic development in memories. For example, bipolar read-write or random-access memory (RAM) chips have advanced as follows:

Year When First Widely Available	Number of Bits
1969-70	16
1971-72	64
1973	256
1975	1024
1977	4096

Cost reductions have paralleled bit density increases. A consequence of higher density RAM technology is that cache memories are now extensively used in mid- and upper-range minicomputers. Bipolar ROM densities have led RAM densities by about a year. Thus, the 2048-bit ROM, organized as 512 x 4, was available in 1975.

These factors have made microprogrammed control increasingly attractive to the minicomputer designer. While large scale computers utilized extensive microprogramming during the 1960s, it was not a cost-effective choice for the minicomputer designer because of the prohibitive cost of the read-only storage technology then available.

Both hardwired control devices and microprogrammed control devices have curves that trace increases in cost as they implement increasing functionality (see Fig 3). However, the rate of cost increase is less for microprogrammed controls than for hardwired controls. Davidow[2] demonstrates that a factor-of-four difference exists between the two slopes.

At some point, the two related hardwired and microprogrammed curves cross. Beyond that intersection, mi-

croprogrammed controls are more economical to use in a design. Both of these curves are moving downward in cost with time, but the curve for microprogrammed controls is moving downward at a faster rate. Thus, the intersection point of the two curves is gradually shifting in favor of microprogrammed controls because the two technologies are moving at different rates. The PDP-11 family offers an example of this trend. At the time the 11/20 was designed, the crossover point was to the right of the PDP-11 instruction set on the abscissa. Hence, the 11/20 used hardwired controls. However, all subsequent implementations have used a ROM-controlled microprogrammed processor. O'Loughlin[3] contrasts the control implementations of four members of the family.

Instruction decode on the 11/60 provides an example of a different use of ROMs. For the secondary decode (the primary is done by combinational logic), part of the instruction register addresses a ROM in which control-store-address offsets are stored. This data-table approach offers both a component saving and a more systematic design. Another example is a ROM-stored table that inspects memory addresses to detect those which refer to locations internal to the processor.

Other advances in semiconductor technology that have affected the minicomputer designer's task include the development of 3-state logic devices and greater levels of gate integration in logic chips. Widely available in 1975, 3-state logic encourages bus-oriented designs. Six 3-state buses are implemented in the 11/60. Examples are the 48-bit wide control signal bus in the CPU and the 60-bit wide fraction data and 10-bit wide exponent data buses in the floating-point processor.

Increased gate integration in logic chips had its major impact on constant-cost minicomputers when the design evolution moved from the 11/20 to the 11/40. The latter machine made heavy use of medium scale integration (MSI). The MSI available to 11/60 designers had negligible density gains over that available to the 11/40 designers. However, after the basic technology decision for the 11/60 was made, a significant step in gate integration did occur. The bit-slice technology, as typified by the 4-bit wide bipolar AM2901 microprocessor slice, became widely available. A 1977 technology decision for a mid-range minicomputer would clearly choose bit-slice components. For the 11/60, however, improvements came from the introduction of 3-state logic and from availability of a wider range of Schottky logic components.

Three semiconductor technology advances contributed to the 11/60 price/performance design in differing degrees. Most important was the cost reduction in ROMs; next was the density improvement in RAMs, and third was the (minor) increase in random logic density.

Price/Performance Balance

Two components, the cache memory and the medium-bandwidth I/O structure, demonstrate the price/perfor-

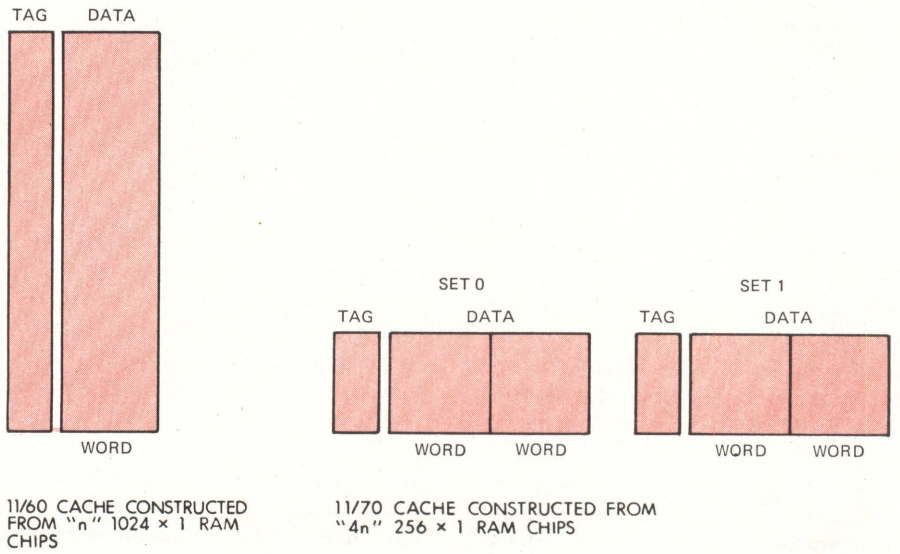


Fig 4 Cache comparison. Simple direct mapped cache of the 11/60 contrasted with the 11/70 cache illustrates a price-performance tradeoff. 11/70 cache has a block size of two (two words are transferred from primary memory) and a set size of two (a word may be placed in either set). Component savings of the simpler organization are clear; only one address comparator is needed, no multiplexer is required to select the output of the data store, and only one set of parity checkers is needed. Hit ratio of the simpler 11/60 cache is 0.87 as compared with 0.93 for the 11/70 cache, which required five times the component count

mance balance characteristic of the 11/60 mid-range minicomputer.

Cache is now a well-proven technique in computer memory implementation. Its purpose is to achieve the effect of an all high speed memory by using two memories—one slow (primary) and one fast (cache)—and by taking advantage of the fact that most of the time, data being used are in the fast or cache memory. Programs typically have the property of locality; that is, over short periods of time, most accesses are to a small number of memory locations. The hardware algorithm managing the cache attempts to keep copies of these locations in the cache. The term "hit ratio" is used to describe the proportion of requests for data or instructions which are satisfied by reference only to the cache. Alternatively, "miss ratio" is the complement of hit ratio. Performance is determined by the hit ratio, which is a function of several cache organizational parameters, including (a) cache size, (b) block size (amount of data moved between the slow or primary memory and the cache), and (c) form of address comparison used.

Strecker[4] describes the research which led to the use of a cache memory in the 11/70. His simulation models were also used in the 11/60 design. By comparing the designs of these machines, several tradeoffs made to obtain a lower cost memory system appropriate to the mid-range 11/60 can be noted.

First parameter to be determined was the amount of data to be moved between primary memory and cache. This decision was closely related to the width of the internal memory bus connecting I/O devices to primary memory. Since the 11/70 was planned to support several high speed direct memory access (DMA) devices, eg, swapping discs operating concurrently, its designers provided a 32-bit bus to memory to supplement the 16-bit wide Unibus. Because the target 11/60 users do not require such a large I/O bandwidth, the Unibus is used for DMA traffic. The 11/70 cache has a block size of two 16-bit words and transfers 32 bits from memory to cache across its dedicated memory bus. Since the 11/60 uses the 16-bit Unibus as its memory bus, the simplest block size—one 16-bit word—was chosen. Note that a 2-word block size can be achieved with a 16-bit bus; the bus is cycled twice to effect a 2-word transfer. Cache simulations showed that this bus cycling would raise the hit ratio of the 11/60 from 87% to 92%. However, the associated performance gain was judged not to be worth the significant added cost of the extra control logic needed to cycle the bus twice.

The next decision concerned the size of the cache. Simulation results showed that the miss ratio decreases rapidly for cache sizes up to 1024 words and less rapidly for larger sizes. But how should the 1024 words be partitioned? Because a full-associative cache requires an expensive content-addressed memory, the partitioning choice for minicomputers is that for a set-associative cache. Since a complete discussion of associativity and replacement is beyond the scope of this article, the reader is referred to the papers by Meade[5] and Strecker[4].

Degree of associativity and total cache size were dominated by the form factors of two candidate RAM chips (256 x 1 and 1024 x 1). These factors are illustrated in Fig 4. The following list shows the clear price/performance advantage of the chosen 1024-word, set-size-of-one cache.

RAM Chip Capacity	Set Size	Cache Size	RAM Chip Count	Hit Ratio
256 x 1	1	256	n	0.70
256 x 1	1	512	2n	0.75
256 x 1	2	512	2n	0.82
1024 x 1	1	1024	n	0.87
256 x 1	2	1024	4n	0.93
1024 x 1	2	2048	2n	0.93

Resulting structure is shown in Fig 5. This simple, direct-mapped organization should dominate minicomputer cache designs in the near-term future. By using the design evolution model shown in Fig 1, it is projected that the two candidate RAM chips for the successor to the 11/60 cache will be the 1024 x 1 and 4096 x 1 chips. Obviously, the design choice for that new class of machine will be a 4096-word direct-mapped cache.

Since simulation data show negligible performance difference between various write-allocation strategies, the lowest-cost strategy, that of allocate-on-write, was implemented. Because the 11/60 utilized a set-size-of-one cache, there was no need to decide upon a replacement algorithm. The 11/70 uses a random-replacement algorithm.

Next decision to be made concerned placement of cache. Two choices were evaluated. The cache could be placed between the Unibus and the primary memory, or between the Unibus and the central processor. The latter was chosen because of these advantages:

(1) Machine execution is faster since the high speed cache is local to the central processor. Time delays associated with synchronization and transmission on the Unibus are avoided.

(2) Instead of designing 11/60-specific memory modules, existing memory subsystems which interface to the Unibus could be used. Moreover, as faster Unibus-interfaced memories become available, they can be installed on the machine without change.

(3) DMA traffic interferes with processor activity to a lesser extent. DMA activity takes place over the path labeled ABC in Fig 2. Processor speed is degraded by interference with I/O operations only when the cache needs to reference the primary memory, using path ABD in Fig 2. This happens only in the event of a read miss, typically less that 13% of the time, and on write operations (10% of memory references).

Disadvantage of this placement is that a mechanism to monitor DMA traffic must be added to the cache to avoid the "stale data" problem. (When the processor reads a location which has been written by DMA, it must receive the information from primary memory.) The alternative placement avoids this extra mechanism by handling both DMA and processor requests with the same mechanism. However, there is more interference between the processor and I/O activity.

Increased memory chip density and the cache performance tradeoff resulted in a significant component reduction. The 11/70 cache occupies four printed circuit boards (approximately 440 chips); the 11/60 occupies less than one board (approximately 85 chips). This factor-of-five component reduction is due to: (1) absence of the 32-bit bus, (2) simpler cache organization, and (3) semiconductor technology advances; these three factors contributed in approximately equal proportions.

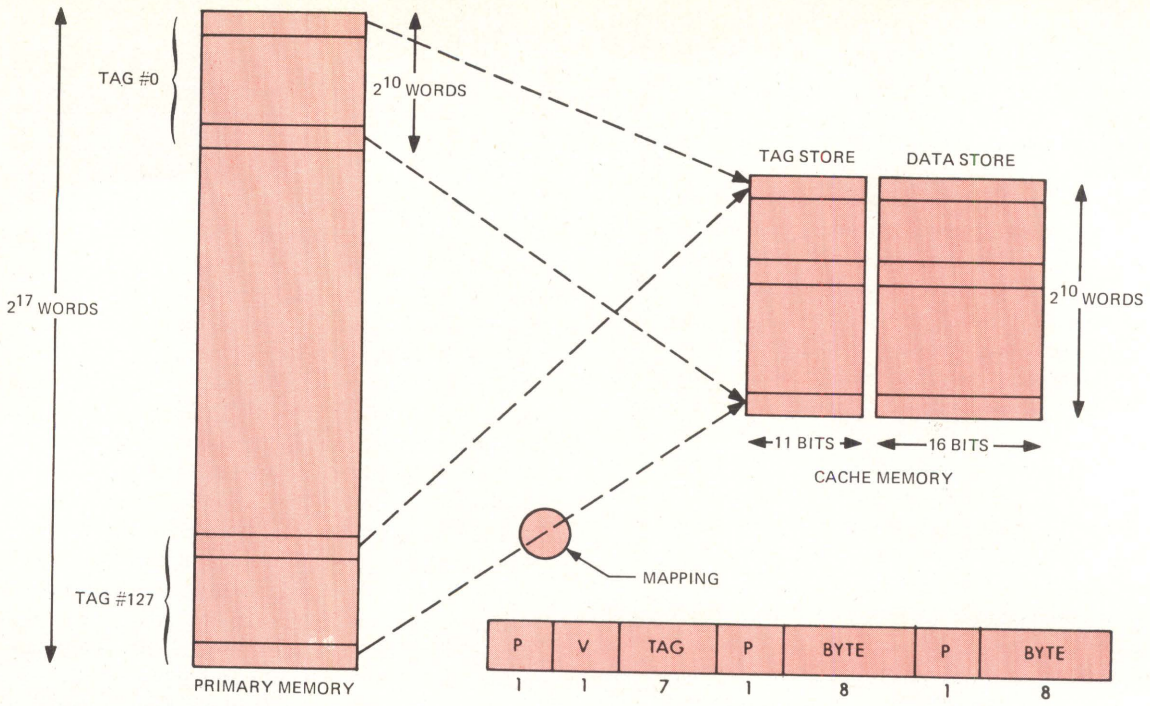


Fig 5 Direct mapped cache. Mapping occurs from 128k words of primary memory to 1024-word cache. High order seven bits of an 18-bit address are stored in tag store to ensure uniqueness in mapping. Tag store also holds a valid bit and parity bits. Cache word format (27 bit in total) is as shown in the bit map

Frequency Driven Design

Because the 11/60 implemented a stable, mature instruction set, several years of programming experience were incorporated into the system design. A simulator program was used to gather execution statistics on a range of programs. Frequency distributions of operation codes and addressing modes drove the design of the base 11/60 and the floating-point processor option.

Functions implemented in hardware, as opposed to microcode, require less time to execute. However, microprogrammed implementations are less expensive, as shown in Fig 3. Frequency distributions of operation codes guided the tradeoff. A balanced mixture of hardwired and microprogrammed implementation of functions produced a central processor that approached the speed of a computer with completely hardwired control functions, but at a lower cost.

Frequency distributions of floating-point operands were also used. Sweeney[6] analyzed the execution of more than one-million floating-point additions and tabulated the behavior of preshift alignment and postshift normalization. Both distributions are highly skewed toward low numbers of shifts. By exploiting these data, the floating-point processor performs a double-precision add in 1.02 μs as compared with 1.68 μs on a comparable unit that uses a conventional algorithm.

To measure the price/performance advantage claimed for the frequency-driven design approach in the base 11/60, a similar machine was needed for comparison. Obviously, such a machine, realized in the same semiconductor technology and designed so that the hardware resources were divided equally among all instructions, was not available. However, data were available on floating-point implementations. The floating-point processor design was a four printed circuit board unit which exploited the frequency distributions of operation codes, addressing modes, and shift amounts. A theoretical comparison was made with another 4-board design which did not use a frequency-driven approach. The 11/60 floating-point processor was estimated to exhibit a performance gain of 30 to 40% on the standard set of benchmark programs used throughout the design process.

Integral Floating-Point Arithmetic Unit

Addition of an integral floating-point arithmetic unit to the 11/60 was a direct consequence of market feedback. In particular, it was determined that the majority of the machine's users would use FORTRAN IV as a source language. In addition, among those using that language, many were not interested in heavy floating-point computation because integer arithmetic dominated their applications.

The FORTRAN IV-Plus compiler has been optimized for execution speed (as opposed to compile speed)—typically a factor of three over other available FORTRAN IV compilers. This compiler, however, employs the instruction set and auxiliary registers of the PDP-11 floating-point

processors. Thus, to take advantage of the compiler's efficiency without burdening the user with the cost of a fast floating-point processor, the central processor must provide those floating-point instructions. This is done by emulating the 46 instructions, including the 64-bit data operations, of the full floating-point instruction set using the 16-bit wide data path of the base 11/60. For users who require FORTRAN IV, but have low floating-point content in their programs, the integral floating-point unit is all that is necessary.

Additional microcode and register space added a few percent to the CPU cost. However, for that small cost increase, FORTRAN IV performance on integer programs was increased by 300%—a dramatic increase.

Cabinet-Level Integration

Physical packaging of minicomputer systems involves another set of tradeoffs. Several levels of size integration are available, ranging from the chip level (LSI-11), through the board level (11/04) and the box level (11/34), to the cabinet level (11/60).

At the cabinet level, packaging techniques are generally traditional. System fabrication is frequently the result of determining methods to install subassemblies into standard racks. At this configurator level, generalized subassemblies are usually chosen for certain functions.

This generally evokes a cost. For instance, there may be a great deal of unused space in conventional industrial racks; in most cases this excess space is simply covered with blank paneling. The cooling system, however, must be designed as if all the racks within the cabinet were occupied with subassemblies.

It was projected that the majority of the configurations sold would be system oriented; thus, design optimization at the cabinet level would be worthwhile. Therefore, the standard 11/60 is cabinet packaged. Fig 6 shows how the CPU, memory, disc units, power supplies, and expansion backplane are packaged to gain the advantages that stem from cabinet-level integration. This integration also yielded added volume, allowing a more powerful blower system to be installed. Acoustic sound power emittance is very low, considering that the rated operating environment is DEC Standard 102 Class C (122°F) for the processor. Improved power efficiency, appearance for the office environment, and subassembly accessibility are also provided.

User Microprogramming Option

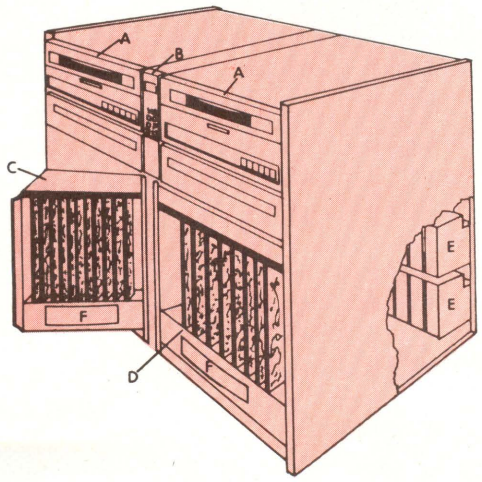
User microprogramming was incorporated in the system to meet growing market demands. The option allows users to create instructions that tailor the central processor, particularly the data flow, to his particular application.

Many potential applications of microprogramming were considered during the design of the data path and control sections of the 11/60. They ranged from instruction set extensions, eg, translation, string, and decimal arithmetic operations, to application kernels, such as node manipulation in list processing and fast Fourier transform in signal processing. Merely substituting RAM for ROM control does not result in a microprogrammable computer. A microprogrammable computer system should have the following:

(a) Extra address space in the control store
(b) Generality in the data path's processing elements
(c) A means to load the writable control store (WCS)
(d) User-oriented hardware documentation
(e) Software to support writing and debugging microprograms
(f) Integration of hardware and software protocols

All these capabilities were designed into the 11/60 WCS option.

A previously reserved operation code, 0767XX in the PDP-11 instruction set, has been allocated for users. Its designation is XFC, extended function code. When this code is recognized, the CPU transfers control to the upper 1024-word block of the 4096-word microprogram address space. User-written microcode may take over from there.



LEGEND:
A-DISC DRIVES
B-MAINTENANCE CONSOLE
C-CARD CAGE SWUNG INTO MAINTENANCE-ACCESS POSITION
D-CARD CAGE IN CLOSED POSITION
E-REAR ACCESS MODULAR POWER SUPPLIES
F-BLOWER SYSTEM

Fig 6 Cabinet packaging. Primary design goals were reliability and maintainability. System logic is mounted on swing-out card cages (C and D) for easy access. Rear access power supplies (E) are modular. Cable routing reduces electrical noise and crosstalk. Blower system (F) keeps all devices cool. Keypad (B) with numerical display facilitates machine control and maintenance. Discs (A) are top or front loading units

A second (asynchronous) type of entry to user's microcode is also provided. This occurs when a WCS-serviced interrupt is recognized by the base machine. Thus, a user can write interrupt service routines in microcode and invoke them without the usual interrupt overhead. Such routines may even be complete I/O channel emulations.

Implementation of the basic 11/60 demonstrated flexibility of microprogramming. The techniques were used in such diverse functions as console service, error logging, floating-point arithmetic, and cache initialization.

Microprogramming does not always result in significant performance gains. Well-suited applications can gain by a factor of five; poorly suited ones may give only minimal improvement. This is supported by measurements on digital signal processing software reported by Morris and Mudge[7]. Prospective users must carefully analyze the execution behavior of the application to determine which parts are "hot spots," ie, most frequently executed. For the average application, an overall factor-of-two improvement should be expected. This average, found to be a useful rule of thumb, is derived by assuming that all hot spots are microprogrammed and the remainder of the program is left unchanged.

Two user-microprogramming options are available. The first is composed of the writable control store module, software tools, and associated manuals. The second is a board containing control logic and sockets ready for the insertion of custom programmable-ROMs (P/ROMs) containing microprograms developed with the writable control store. This extended control store (ECS) option is designed for situations where microcode integrity and/or multiple installations are required.

A novel structuring of the writable control store allows it to be used to store data. Availability of data storage local to a processor, ie, not accessed through a main, general-purpose memory bus, can increase system speed. Such local store is usually implemented in some special technology that has low capacity but high performance. Writable control store has been structured so that the 48-bit microinstruction storage words can be read and written as 16-bit data words. In addition to conventional writable control store hardware, logic is available to realize a local store address register (LSAR) and a local store data register (LSDR).

Thus, the microprogrammer has fast local store available. This storage is block-oriented. A 3-cycle overhead is needed to start a block read (or block write); then, words are read (or written) at the rate of one per microcycle. The microprogram can be logically partitioned into two sections: control store—48-bit control words; and local store—16-bit data words (three per microword). A common partitioning would be 512 words of control store and 1536 words of local store.

Reliability and Maintainability

Design decisions to allocate a portion of the cost of the 11/60 to reliability and maintainability, rather than to further improving performance, were motivated by user and market needs. Prime considerations were the increasing labor cost associated with maintenance and the growing use of minicomputers in applications demanding more reliability.

First goal was to increase the mean time between failures (MTBF) by (a) reducing the occurrence and impact of normally fatal hardware malfunctions, (b) providing error statistics, and (c) providing operating alternatives to keep the system running after failures occur, albeit at a lower performance.

Second goal was to reduce the mean time to repair (MTTR) when hardware malfunctions occur, by (a) hardware design and packaging that facilitate error diagnosis and repair during scheduled and nonscheduled maintenance, (b) continuous logging of hardware errors during system operation, and (c) provision of software and microdiagnostic tools for problem isolation.

MTBF

Reducing the incidence of fatal hardware malfunctions was a joint effort by engineering and manufacturing. The Schottky transistor-transistor logic (TTL) used in the machine, having been in widespread use for over five years, is a well-proven family of devices. Moreover, conservative electrical design practices were followed.

Plotted against time, chip failure rate tends to follow a bathtub-shaped curve, high at either end of the life cycle. The 11/60 production process includes extensive thermal cycling to ensure that "infant mortality" cases are discovered early during manufacturing.

The cabinet is designed to minimize buildup of hot air over the processor boards. Power supplies are mounted at the rear of the cabinet, away from the logic, so that radiant heating effects are minimized. A blower system cools the logic card cage by drawing fresh, filtered air down over the printed circuit boards such that no board receives exhaust air from another.

Other physical packaging to reduce hardware problems include cable troughs, impact-absorbing casters, and special cabinet grounding. A filter is attached to the maintenance console to reduce electrostatic noise interference.

Console microcode double checks every entry to verify data received from the keypad. A significant proportion of the 11/60 microcode (see Table) is devoted to logging microlevel state upon the occurrence of a detected error. This logged state can be accessed via a maintenance examine and deposit (MED) instruction. Logged information is used by an operating system to compile error records, which aid in tracking down intermittent errors.

To reduce the impact of hardware malfunctions on the user environment, a number of fail-soft capabilities have been implemented.

(1) If the cache fails, it is turned off and the still functioning primary memory is used to keep the system running.

(2) If a parity error occurs in WCS, the processor disables that control store. Then, the operating system is notified, and program execution can continue using the basic PDP-11 instructions.

(3) Systems can be programmed to fall back onto the integral floating-point unit if an error is detected in the floating-point processor.

(4) The bootstrap loader permits system loading from an alternative device if the primary bootstrapping device is disabled.

Control Store Usage by Category

Category		Number of Microwords	Percentage of Total
A	PDP-11 Instruction Set		
	Initialization	95	4
	Operand fetch, execution, and operand store	515	20
	Infrequent intraprocessor transfers	230	9
		840	
B	Integral Floating-Point Instruction Set	1010	40
C	Reliability and Maintainability		
	Error logging, MED, and cache fail-soft	190	7
	Console, boot, and initial diagnostic	230	9
D	Support of Options		
	Writable control store	60	2
	Floating-point processor	80	3
E	Reserved for Future Changes and Additions	150	6
		2560	100

Total address space for microprograms is 4096 words, of which the 2560 categorized in the table are implemented in ROM. Note also the increased utilization of microprogramming in the 11/60, as compared to the 11/40.

Category A, totaling 840 words, was implemented in 256 words for the 11/40. The two machines have comparable microword widths. The third subcategory in Category A illustrates the use of microprogramming in the frequency-driven design approach. Examples of infrequent intraprocessor transfers are error handling and data transfer to and from internal addresses, eg, memory management relocation registers.

One of the benefits of a microprogrammed implementation of control is the ease with which engineering change orders (ECO) can be implemented. Space in Category E is reserved for such use and for the further correction of undetected errors in the microcode itself.

MTTR

Error diagnosis is the most time-consuming problem facing the field-service engineer. Special diagnostic tools, both hardware and software, have been designed to reduce the time spent in error isolation.

Focal point of the hardware maintainability effort is the microdiagnostic unit. This single board tests the logic on five of the six processor boards. When faults are detected, an error code is displayed on light-emitting diodes (LEDs). A fault directory can then be used to determine which boards are to be replaced. The unit requires only a small portion of the internal machine (the microword sequencing) to be operational.

In addition, a number of onboard diagnostic aids are included in the CPU design. These include LEDs to display the contents of the next microaddress register, a single-step mode, and a microbreak function.

Software diagnostic programs are used to diagnose errors in system peripherals as well as in all CPU subsystems, such as memory management unit and cache. User-mode diagnostic programs allow peripheral diagnosis to occur while the system is available for other users. Conventional standalone diagnostic programs can also be used.

Physical packaging facilitates quick repair. Hinged card cages and modular power supplies allow easy access and module change.

Summary

The design of a mid-range minicomputer has been used as a concrete illustration of tradeoffs made to effect a price/performance balance. Designers use technology advances, eg, doubling of density on a memory chip, to produce new designs in one of two design styles: constant-cost, increasing-functionality or constant-functionality, decreasing-cost. Increased use of microprogramming, a factor-of-three in this case study, is a trend that was observed.

By choosing a less powerful cache organization, the 11/60 design obtained a factor-of-five component reduction. Cache design also illustrates how some design parameters are highly interdependent. The frequency driven design approach used on the floating-point processor can lead to a 40% performance gain.

Examples of added functionality in the constant-cost style of design include greater reliability and maintainability, and user microprogramming.

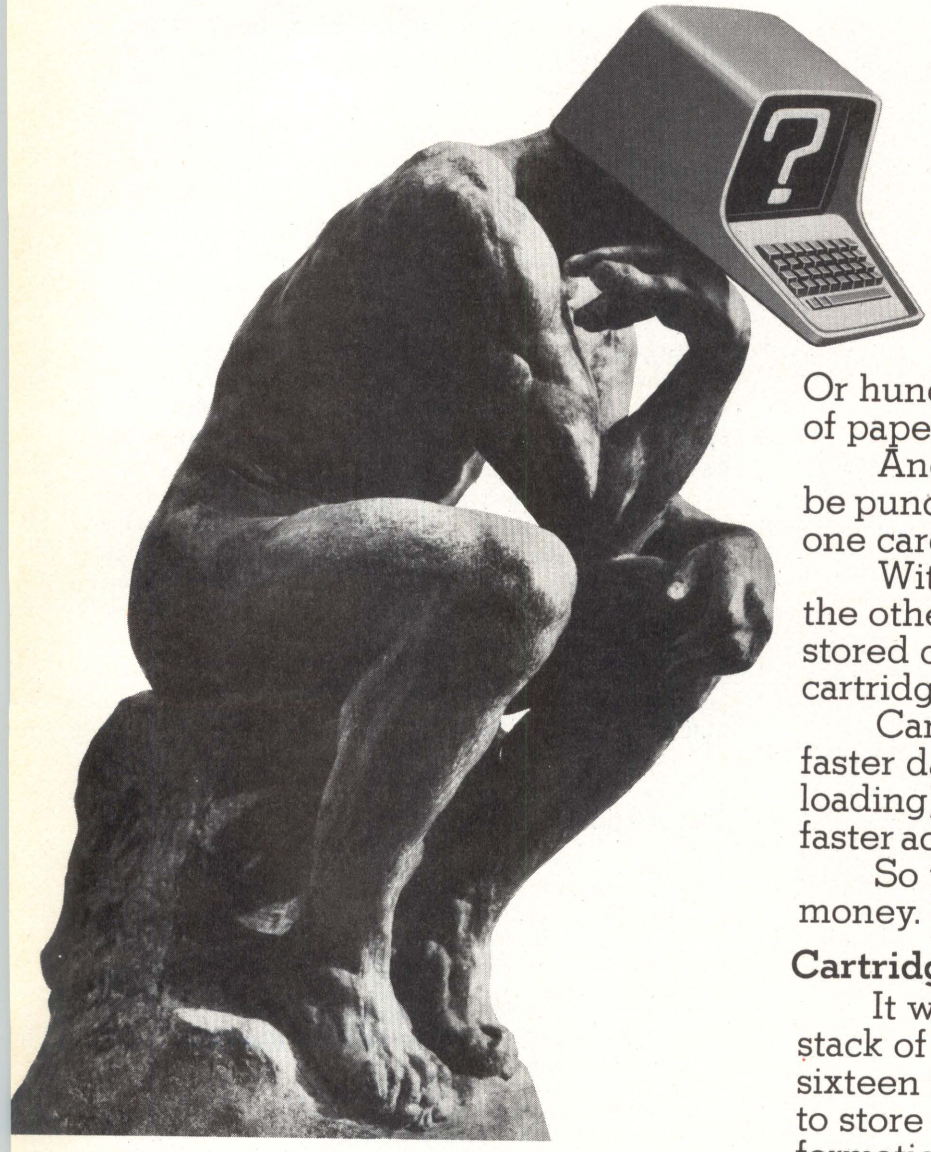
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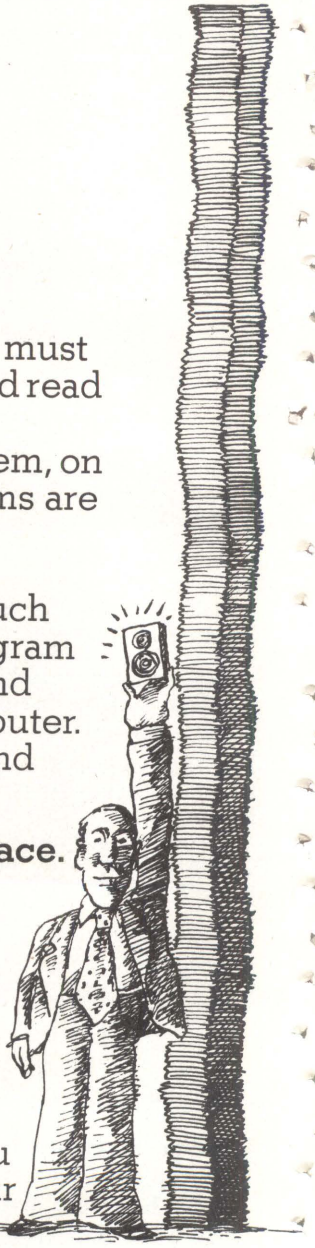


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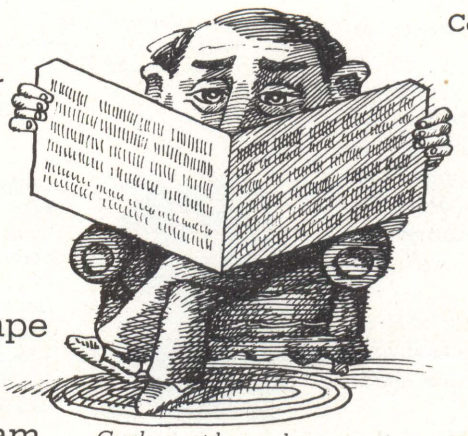
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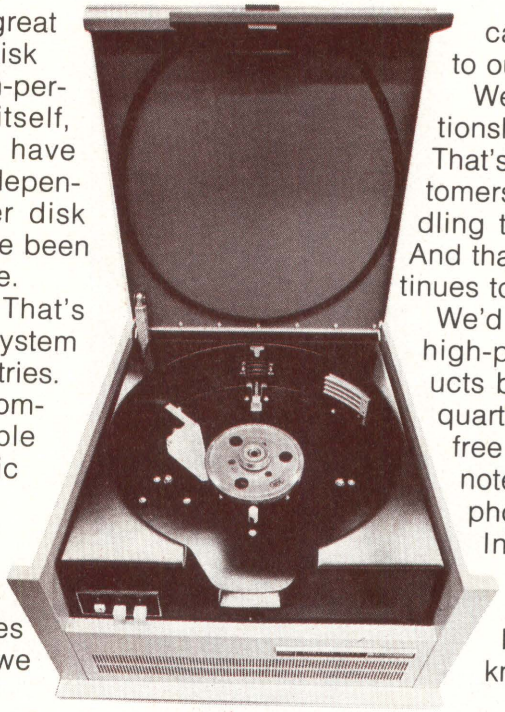
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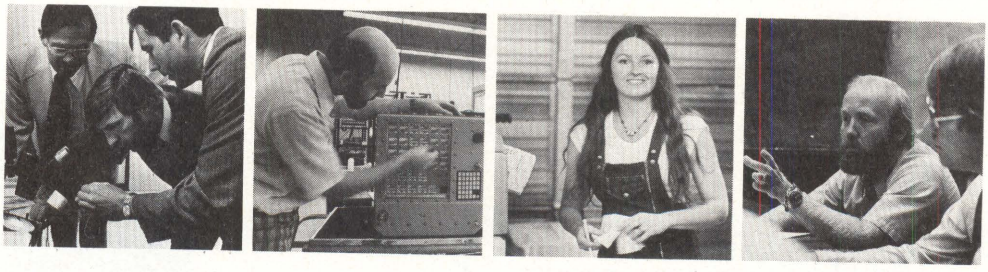


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CIRCLE 51 ON INQUIRY CARD

To realize the profit potential of off-the-shelf standardized software in masked ROMs, microcomputers need a hardware addition to relocate addresses as necessary, leaving the prestructured programs unchanged

Solving Mass-Produced ROM Programming Problems With Base Registers

John A. Carroll

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Software, like most products, is cheaper when it is mass-produced. In microcomputers, however, the programmer who tries to achieve economies of scale is frustrated by traditional architectures adapted from larger computers, where the limitations of read-only memory were never considered. The bottleneck lies mainly in the realm of hardware, and can be attacked most efficiently with a hardware solution—the addition of a set of base registers.

Mass production achieves low unit costs by turning out large runs of identical products. In the case of microcomputer programs, which are often turned into read-only memories (ROMs), the obvious way of carrying out mass production is to process great numbers of ROMs with identical contents. The stumbling block in the path of this approach is the prevalent method of linking various pieces of software together into a complete system, which demands many address changes in each segment. Base registers provide a hardware facility that relocates addresses as needed during execution, making it unnecessary to change them within the program. These registers can be designed into the central processor unit (CPU) chip, or added on by the system builder. The result is the creation of a mass market for standard software.

Nature of the Problem

To see where base registers fit in, a critical examination of the economics of computing and the nature of programming is necessary.

Rapid development of microprocessors, semiconductor memories, and interface chips, and the recent advent of complete packaged microcomputers have brought the minimum cost of a useful computer down to unheard-of levels. This drive to cut costs has resulted in simpler machines that are much easier to interface with external devices. The result is that computing is becoming affordable for more and more applications. Products of all kinds are gaining the versatility of local intelligence, or becoming less expensive, or both.

Unfortunately, the cost of software, and program development in particular, has not kept pace; if anything, the cost has increased. Therefore, the adaptability of computer-controlled machines remains largely potential, because any software change needs to be applied to many machines in order to be cost-effective.

One major reason for this is that big-computer thinking still permeates the methods of microcomputer software production. For example, phases of assemblers and compilers are loaded into read/write memory from

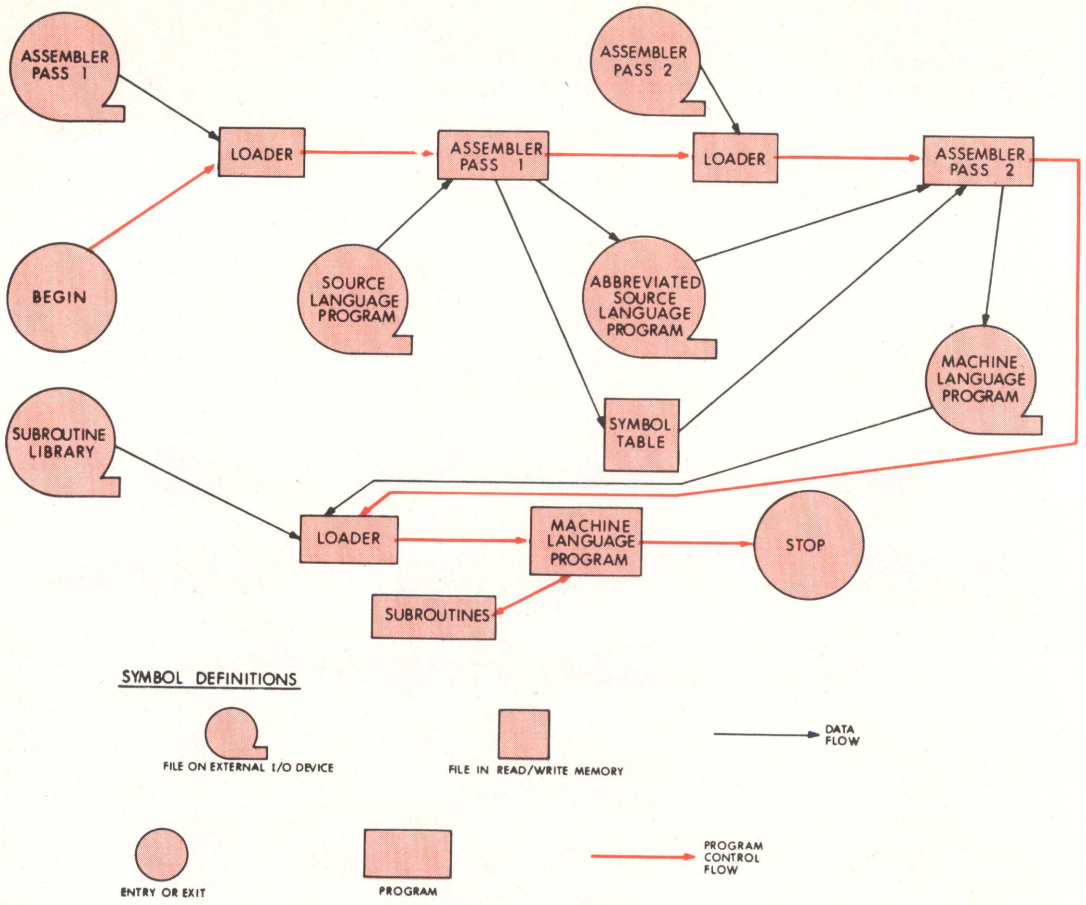


Fig 1 Traditional architecture. Assembling and running program with traditional architecture requires reading in six files and writing two. It is assumed here that loader stays in memory during assembly; otherwise additional reads would be required

an input/output (I/O) device; then, source language is read from one device while partly processed output is written on another. Subroutines are read in from another device, and addresses are altered (relocated) so that all the code needed to run a job fits together in memory with no wasted words between. This loading process is diagrammed in Fig 1.

While this approach to programming may have made sense in the days of the IBM 1401, when memory was prohibitively expensive and all read/write, and large quantities of fast I/O were necessary to handle large files of data, microcomputers are different. Memory costs have dropped considerably and ROM is roughly 10 times cheaper than any other kind. Moreover, memories are now available in very small capacities at low prices. In addition, microcomputers are being used in many direct-control applications that require no writing or rereading of data. Thus, in many cases, program development is the only reason for having a conventional I/O device. The devices themselves (cassette drives, floppy discs, teleprinters) are often either much more expensive than the computer, or painfully slow, or both.

Available alternatives are to use a timesharing system with adequate facilities, to use a well-equipped microcomputer development system that approaches a minicomputer in both capability and cost, or to do most of the software work manually if the program is simple enough. Clearly, something is out of balance.

Solving the Problem with ROMs

ROMs are widely used in small computers for several reasons. First, they are the cheapest means of storing information that is not going to change, unless the quantity of information is so large that the cost of ROM equals that of some machine like a floppy disc. Second, having the information permanently in the computer does away with the need for loading when the system is turned on. These two considerations eliminate I/O devices from many microcomputer installations, and greatly reduce system cost. In addition, reliability and convenience are enhanced with the physical impossibility of altering or losing a permanent program. Therefore,

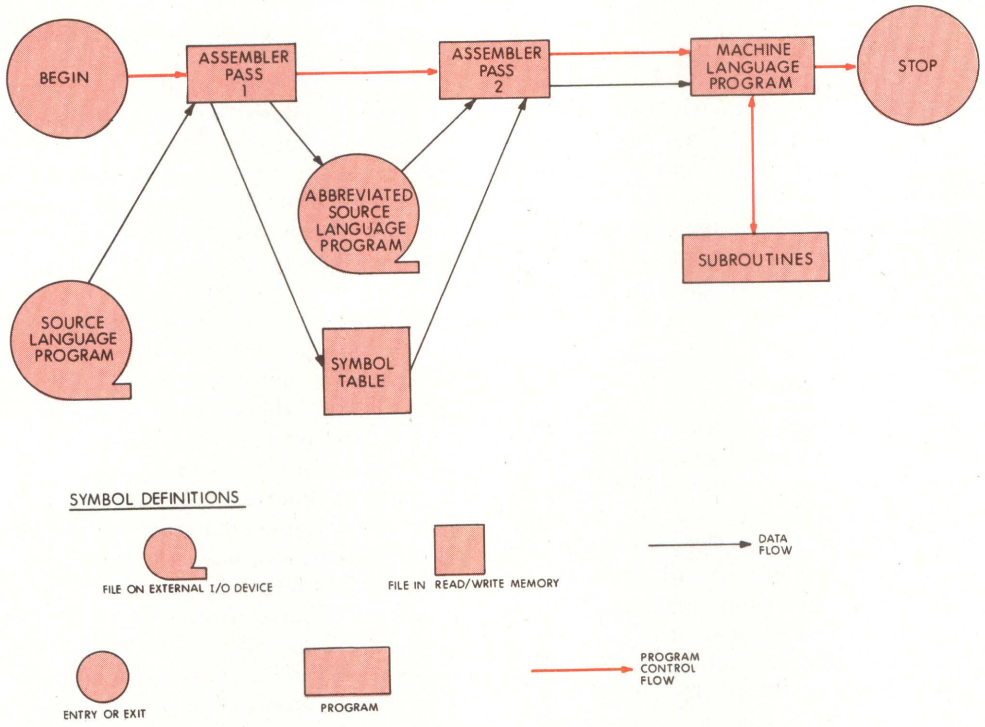


Fig 2 ROM-resident software. Assembling and running program when all system software is in read-only memory (ROM) requires reading only two files and writing one. Abbreviated source language program is normally much shorter than assemblers and library that no longer need to be read. Handling and actual read time are both reduced by roughly 70%

an efficient method of programming microcomputers must take into account the use of ROM.

Two powerful timesavers are available to the programmer in the form of standard software—language translators and subroutine libraries. The former translates a readily understandable programming language into the machine's own internal code, while the latter is a set of off-the-shelf program fragments that perform commonly required functions. They are the programmer's equivalents of large-scale integration (LSI). Fig 2 illustrates the simplifications that result from putting standard software into ROMs.

Since most subroutines have internal jumps and external references, a number of actual machine addresses need to be filled in before use. To do this, the normal technique is to read the routine into an available area in a read/write memory under control of a small program called a relocating loader, which keeps track of where in memory everything is and calculates actual addresses needed in various instructions.

Putting all standard software into ROM would result in many practical benefits. In many systems, most of the data-juggling programming could be inside subroutines, leaving only a relatively small application-oriented program to direct the whole task. Most software could be selected from a catalog of standard, factory-programmed ROMs, and just plugged in.

This method is better than reading in the same software from a tape and relocating it to fit in with the application program, because only a small part of the system needs to be stored in a custom ROM. The remainder can be in a standard mass-produced ROM, instantly available, and free of bugs. Reducing the volume of material to be read in reduces demands on I/O equipment; in many cases, program development with nothing more than a teleprinter becomes a reasonable proposition.

There are other benefits. Having all this software in ROM eliminates the need for random-access semiconductor memory (RAM) to hold it during the development stage—and RAM costs more than ROM. In many systems, great ingenuity is applied to minimizing the amount of software that needs to be in memory simultaneously, to enable the use of a smaller memory. Storing software in ROM does away with this whole

problem, resulting in a simpler software system and eliminating the time lost when the next part of the program has to be loaded in.

In summary, the system builder benefits from having standard subroutines in standard ROMs, because fewer ROMs in the system need to be custom-made. This can open markets for smaller numbers of identical systems. Additional benefits are derived from having program development software in standard ROMs, because the software system can run in this form with little extra hardware. Program development ROMs can be shipped with the product to make a low cost data processing computer as soon as low cost I/O devices appear. Service personnel also benefit from having diagnostic software in ROM form. It allows them to exercise a defective computer, since the ROM can still be plugged in and used regardless of dead I/O logic.

The Catch

There is, however, a fly in the ointment. Nothing in a mask-programmed ROM can be changed to make all parts of a software system fit together. Remember, though, that many addresses in a program, particularly in jump instructions, assume a knowledge of where in memory each program is located. The whole catalog of software available for a particular microprocessor would quickly exceed the maximum amount of memory its address word could handle; therefore, each subroutine cannot be assigned permanently to a particular block of space. Even if that were possible, many mathematical and data manipulation subroutines must be informed each time they are called just where their data are, and various parameters often need to be specified. Subroutines that handle the details of running an I/O device are often used to run several identical machines, and are told which one by pointing to a memory address that is actually an I/O control register. Therefore, even if software can be relocated for each system and custom ROMs can be fabricated cheaply, or more expensive field-programmable ROMs (P/ROMs) can be incorporated, the fact that external references actually change while the program is running interferes with a software solution.

It follows, then, that the situation described calls for a hardware method of modifying addresses at run-time while leaving the programs unchanged—invariant code, to use the technical phrase.

The Escape Hatch

Here is where base registers come in. A base register is a hardware device that stores an address word, called a base. The base can be added automatically to the address in an instruction before accessing memory, as shown in Fig 3. This capability enables any block of code to be written as if it began at address zero, and the ROM to be wired so that the code can appear anywhere in memory. As long as the program's actual address origin is placed in the base register before execution, instructions within the program can refer to each other correctly. This technique makes it possible to manufacture great numbers of ROM copies of subroutines or programs, all alike, without knowing what address space will be assigned to them in different systems.

Computers that use base registers usually contain more than one. External references can use base registers also; an application program can order a floating-multiply, for example, to act on any two desired memory locations. I/O routines can use base registers to point to the pseudomemory location that actually accesses the I/O device as well as to determine the memory area where the read or write is to occur. The latter function will require at least two base registers. Having several allows different registers to be assigned to different functions, thus reducing the need for reloading them. Even a non-ROM application program can benefit from base registers. I/O routines can read and write in one set of work areas while the program processes data in another, and extra registers can direct the application program.

Normally this hardware is managed by allocating several bits of the address word for selecting one base register out of a set. The remaining bits are then added to the contents of the chosen register. The sum is sent out on the address bus to actually select a memory word (or some piece of hardware wired to the memory address decoder). Thus, the address word specifies a location that can be offset by a considerable amount from the base to permit jumps or memory access throughout a reasonably large section of memory without changing the base. In Fig 3, the most significant four bits of a 16-bit address word have been assigned to base register selection.

A certain amount of housekeeping software makes it easier to run a computer with base registers. If some addresses are not subject to relocation, this software is easier to write and the turn-on process is simplified. Therefore, one base register selection code is defined as "no base register," providing some space down at the bottom of memory assigned to system functions. Since the amount of memory that can be reached without changing bases is often called a "page," the no-base region is called "page zero."

All of these techniques became well-known with the advent of the IBM System/360 where, although they added some convenience and efficiency, they did not really add any new capabilities to an all-RAM machine. Perhaps the association of these techniques with big machines, combined with the drive for hardware simplicity, has caused base registers to be overlooked for microcomputers, where they can lead to economies that are otherwise impossible.

Adding Base Registers

One of the most interesting aspects of a base register network is that it can be retrofitted to almost any computer. The network does not have to be designed into the chip, although there are inherent advantages in doing so. Only three ingredients are needed—a reasonably fast memory of a few words that is as many bits wide as desired in the final, processed address word; an adder as wide as the memory; and a little steering logic.

Fig 4 shows the elements of a simple base register add-on network. This illustration is intended to present the discussed principle; obviously, other implementations are possible.

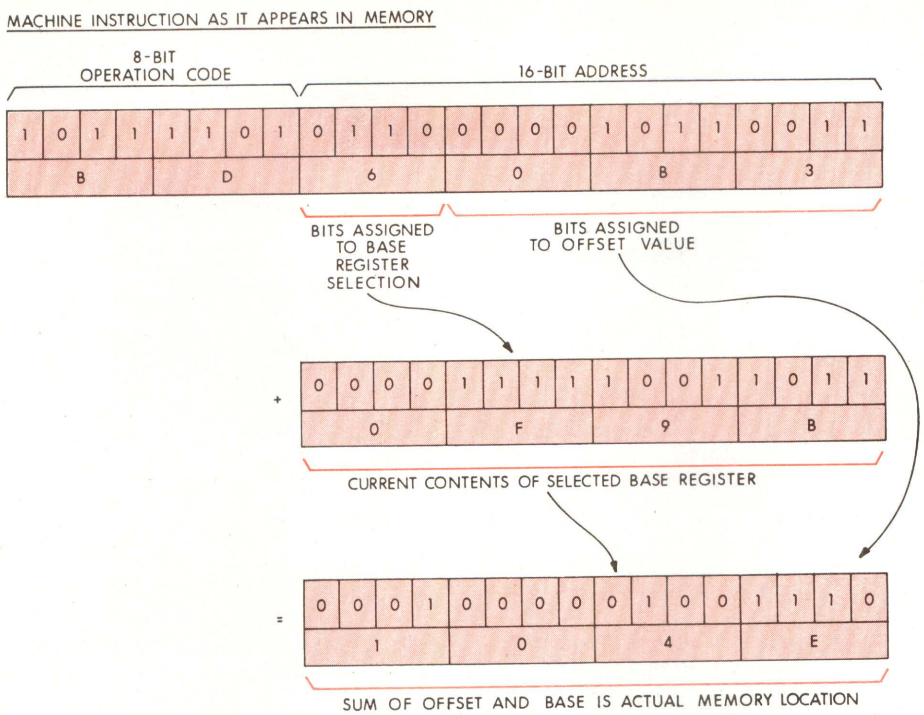


Fig 3 Base register operation. In this example of base register operation, as seen by programmer, content of each register and bus is shown in both binary and hexadecimal notation. Typical 3-byte machine instruction, appearing in program memory as BD60B3, consists of 8-bit operation code BD and 16-bit address 60B3. Without base registers, location 60B3 would be accessed. However, machine represented here has been augmented so that the 6 causes register 6 out of a set of 16 to be read out. Some previous operation has stored value 0F9B in this particular register. Rest of address, 0B3, is still used as an address value, but indirectly; it is added to contents of register 6. 0B3 + 0F9B = 104E. Instruction then accesses location 104E

Since 16-word memories are readily available and 16 registers is a convenient set size, it is reasonable to use two 16-word, 8-bit memories. The two memories are combined to obtain a 16-bit-wide memory that interfaces with the 16-bit address bus typical of microprocessors.

In operation, the four most significant address bits from the CPU, A12 to A15, propagate through the multiplexer to select a word in the base memory. This 16-bit word goes to one input of the adder. The least significant 12 bits, A0 to A11, are the other input. The sum is the relocated address, which controls the main address bus that operates the rest of the computer. As long as these elements have a reasonably fast propagation delay, the system clock can run almost as fast as if the base register network were not included.

Note gate B in Fig 4. When bits A12 to A15 are all 0s, this gate is disabled. In turn, gate B disables the 16 gates at F, and the outputs of these gates force all 0s on the base input to the adder. In other words, if the base selection code is 0, the base register output value is 0. This override function gives the system housekeeping software guaranteed access to nonrelocatable items in page zero, even though the content of the base registers may be indeterminate. This is a convenience in calls between programs, and is practically indispensible in getting the system started when power is first turned on.

However, a data path is needed for loading the base registers. The 16 x 16 memory is divided into two 16 x 8 sections so that each section of memory has its input connected to the 8-bit data bus. To address memory for loading, a block of 32 locations is assigned in page zero. Gate A recognizes some specified configuration of bits A5 to A15. (Since A12 to A15 are all 0s when page zero is being addressed, an input to gate A can be tied onto gate B without decoding these four bits again.) Gate A is enabled with the system write pulse (or whatever equivalent the particular computer has) to synchronize write operation. The output of gate A is the master base register write pulse. This output is gated through either gate C or gate D according to the least significant address bit, A0. This gating action has the effect of giving both halves of a particular base register adjacent locations in memory—certainly the most convenient arrangement for the programmer. Specifically, the most significant half of the base memory must be selected when A0 is 0, so that a base is written "from left to right" (except in the case of the 8080). The remaining bits, A1 to A4, are passed through the multiplexer

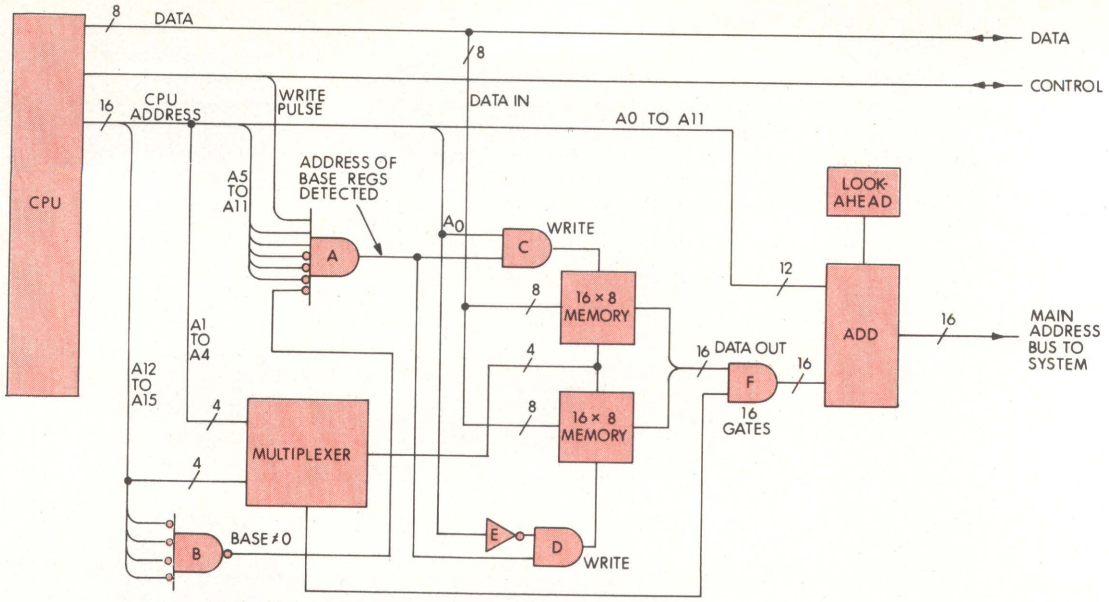


Fig 4 Typical base register add-on. To use off-the-shelf software in masked ROM form, microcomputer needs way to relocate addresses within instructions to their actual machine locations. Set of base registers, in form of two small memories, contains origins of currently active memory areas. Part of instruction address word selects register and adds its contents to remainder of word. For clarity, this simplified block diagram omits base register read capability, increment/decrement logic, and other optional features

to select the word in base memory that is to be written. A lookahead circuit can be connected to the adder to speed up address propagation if necessary.

The network shown in Fig 4 requires a fairly small amount of hardware, and will not add greatly to the support ICs in a typical single-board computer. A small saving in software costs would easily pay for this kind of overhead.

Note that the base register and the adder can have more bits than the CPU's address bus; this simplifies expansion of memory capacity.

Associated Software

Various small pieces of programming are used to coordinate the operation of a computer that has base registers. The whole collection is called the "kernel." It interacts so closely with the hardware that design of the base register set and the kernel is best treated as a single task.

Most important part of the kernel is the "link," an extremely short section of code that allows a program to call a subroutine without having its absolute location written into the calling program. Without a link, a standard program in ROM would not be able to locate a subroutine. With the link, the calling program merely specifies the name or catalog number of the desired subroutine, and the link loads the base of the subroutine into one of the registers. After that, the instruction that calls the subroutine merely needs to have the correct base register specified in its address field.

The link works with a table that describes the actual memory location where each standard ROM program is wired in the particular machine. A p/ROM is a good device for storing this unique table; it is instantly available at turn-on time. If the machine is modified too often to make this approach practical, an unused op code can be defined as a marker, indicating that a program name follows. The power-on routine then can, for example, check every 4096th location and compile a table in RAM of every name found, with the corresponding actual location. The calling program would place the program name in one of the regular CPU registers, and call the link as a subroutine. The link would search the table for a match, replace the name with the location, and return control to the calling program. With the base now in a CPU register, the calling program can not only load it into the appropriate base register, but also can save it in RAM to avoid a search on later calls.

For extra speed, the table could be in a field-programmable logic array (FPLA). This device can recognize a selected few of a very large number of possible bit configurations, which the active program names in the system would be. The program name could be put in a register connected to the "address" inputs of the FPLA, and yield the desired actual location on the output lines in a single access, without a search.

Another typical task for the kernel is to coordinate calls for I/O operations from the main program. This built-in function relieves the program of keeping track of what specific I/O devices are doing, which work areas are assigned to the program, and which are being read or written. The kernel switches these areas around

by changing the bases for the I/O and application programs after each operation. Calling I/O through the kernel also makes it possible to change I/O devices without changing the program—very important when writing a program without knowing what devices the machine will have. A good kernel can provide almost as good a view of the internal workings of a system under development through one of the I/O devices as a control panel would supply.

An orderly plan for assigning functions to specific base registers is important. No two programs on the same system should require the same register simultaneously for different things. There should be a register for the called, or currently active, program; another for a program in the process of giving a call; and at least two each for active input and output routines. This plan leaves some registers for the kernel, a few levels of interrupt, and general temporary storage (the latter if logic is provided to read back a base register).

In some high speed systems, an oversized base memory may be desirable, with some base selection address bits controlled by the current interrupt level. In this case, it is not necessary to save and restore base values on an interrupt. The same can be done for subroutine calls. These functions illustrate the benefits of designing the base register set and the kernel together.

By adding hardware, base registers can be made to increment or decrement after each access; again, two bits in the address word can be assigned to enable this function. This technique could make many I/O and arithmetic routines as much as three times shorter and faster.

Economic Benefits of the Concept

Base registers could provide an economic means that could lead to a thriving market for standard software. Standard software would derive a major part of its value to the user from being in ROM form—nonvolatile, capable of being kept in stock until needed, and then simply plugged in. Software would be embodied as physical parts, used up on a one-per-system basis, just like CPUs, interface chips, and other hardware. It would be uneconomical to copy ROMs in the field, because no other form of memory is as inexpensive as these factory-programmed masked devices. Since a semiconductor factory is necessary to make copies as cheaply as the originals, and then only if enormous numbers are made, a single instance of plagiarism would be too obvious to hide and significant enough to economically justify legal remedies. The user could not economically transfer such software into his RAM for execution because that would increase system cost. It would be even more unattractive for a user to copy standard software onto conventional read/write media and load it in as needed, because that would not only require I/O devices and extra RAM, but also would add the administrative burden of keeping track of a software library.

Thus, the business of writing software as a standard product could become highly profitable. With a mass market, development costs could be amortized over a large number of copies sold, and thus reduced to less than the cost difference between p/ROM and masked ROM. The result would be an economic climate similar to that of the publishing industry, but without the threat of the ever-present photocopier.

Candidates for ROM

What kind of software could go into standard masked ROM? First and foremost are language translators—assemblers and compilers. Also possible are mathematical subroutines, I/O device drivers for commercially available devices, edit and debug routines, software for storage and retrieval of data bases, sort algorithms, instruction set emulators for older computers, kernels, and more elaborate system monitors and operating systems. Anything that a programmer would want to choose from in putting together a complete set of software for an application could be put into ROM.

A sign of things to come is the recent appearance of combination chips that contain both ROM and parallel I/O lines. These chips could serve as a starting point for a complete hardware-software interface to a device—all in one chip.

Conclusion

The base register set may be the missing link which is preventing a complete working microcomputer with practical system software from becoming as available and economical as the hardware itself. Adding base registers will offer the OEM the economy of masked ROM, while enabling the relatively small application program to be stored in p/ROM to respond to the demands of fragmented markets. It will be possible to develop small programs right on the breadboard. As if that were not enough, it should become possible to mass-market standalone data processing systems with sufficiently economical I/O (one method is to include the computer in a common TV set, instead of vice versa) that small businesses and the general public will find the system as useful as the ubiquitous calculator. Therein lies the lucrative prospect of huge sales volume, with the semiconductor industry in a position to reap a large share of both the machine and the software aftermarket.

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An electronics engineer at Dynamic Measurements, John Carroll is involved with analog signal processing modules, power supplies, and microcomputer-related products. His background includes work with A-D converters, servo-controllers, test equipment, and systems software. He holds a BA degree in physics from Occidental College.

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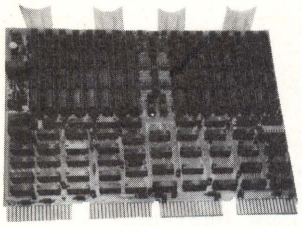
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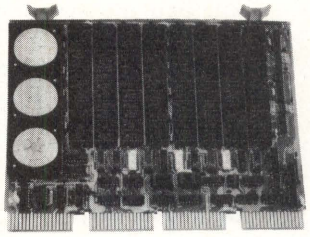
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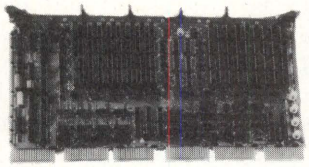
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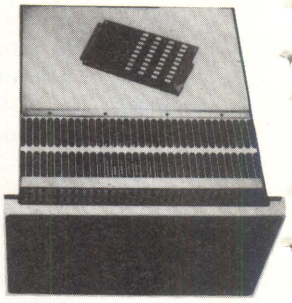
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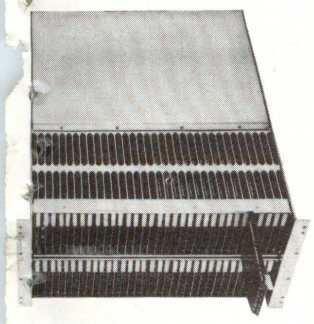
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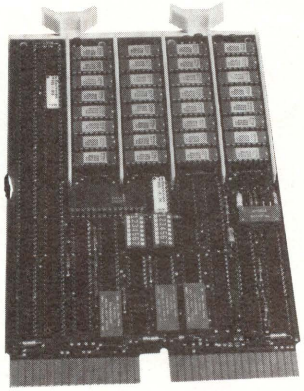
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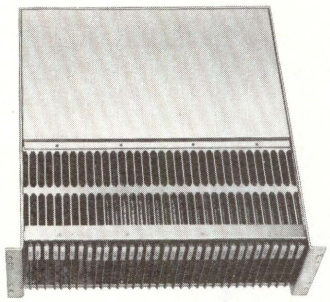
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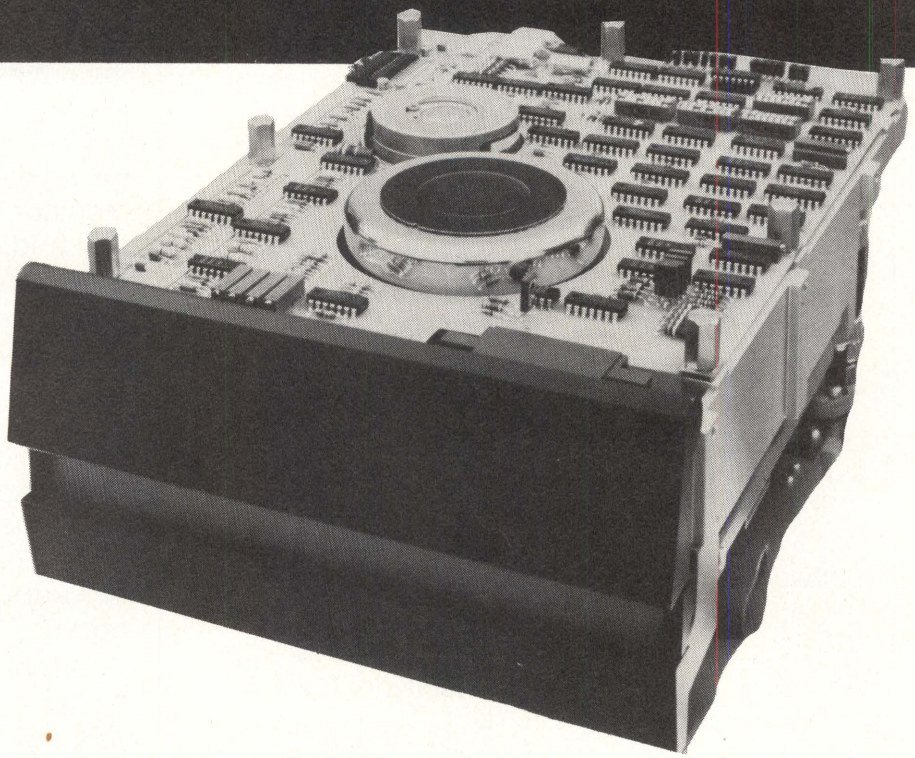
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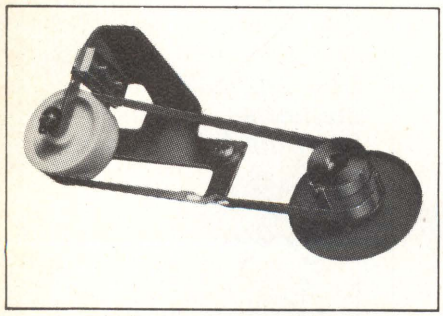
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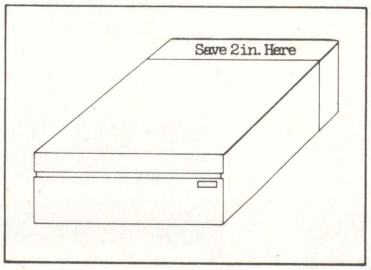
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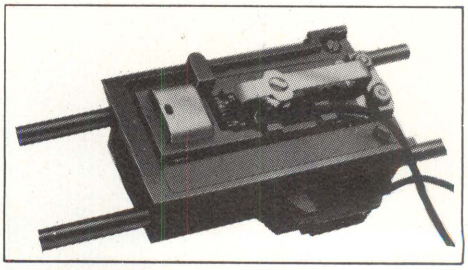
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CIRCLE 59 ON INQUIRY CARD

Cost savings of up to 75% per data channel are realized by a microprocessor-based multiplexer system that solves the 2-way high speed communications problems related to interfacing multiple USART-input terminals to a timesharing host computer

Multiplexer System Reduces Cost of Terminal Interfacing

Austin Lesea and Nishan Urkumyan

University of California at Berkeley
Berkeley, California

A microprocessor-based multiplexer system has been designed to concentrate 32 EIA RS-232-C-compatible terminals onto a single 2-way high speed (9600 baud) transmission line for a timesharing host computer (see Fig 1). Each terminal has buffered output and character-by-character input. Thus, the host computer (in this case, a PDP-11/70) spends less time executing the multiplexing task. This multiplexer system is also applicable, with only code changes in the host machine, for other computers, such as the Data General Eclipse and the Hewlett-Packard 3000-2.

Cost of providing this multiplexing function is $60 per data channel, compared with approximately $250 per data channel for existing commercial designs. Cost-effectiveness increases even more when clusters of fewer than 32 terminals are implemented. Since the multiplexer system has no modem control features, as it is intended to be installed at the terminal site, costs in labor and equipment are minimized.

Using the Intel 8080A microprocessor and 8251 universal synchronous/asynchronous receiver/transmitter (USART) chips provides a programmable serial data channel for the terminals. Presently, three such multiplexer systems are operating effectively at the University of California at Berkeley; two have 32 channels and one has 20 channels.

Design Considerations

Connecting up to 32 USART-input terminals to a timesharing host computer presents the design engineer with the usual communication interconnection problems of interfacing equipment, bus wiring, patchboards, memories, and programming. Initially, remotely located concentrators eliminated most of the interconnection problems. However, since they did not reduce costs, a microprocessor-based multiplexer system design was undertaken to handle the concentrator function at significant cost savings.

Basically, 32 terminals must be processed at an input rate not exceeding 30 char/s, and at the fastest output rate possible. Since 9600 baud is equivalent to approximately 1 char/ms and since the 8080A has an average instruction time of 3.2 μs, input and output (I/O) processing of 32 terminals allocated about 300 instructions/char in the polling loop software routine for the terminals. The host input to multiplexer routine must operate with not more than 200 μs of overhead in order to pick up channel information and still allow enough average time to service the input and multiplexer to host routines. Coding must be programmed in an extremely tight byte-by-byte procedure.

Input is desired at a maximum rate of 15 baud when all 32 terminals operate simultaneously, or at a maximum rate of 4800 baud when only one terminal is used. Minimum desired output rate is 300 baud for all 32 terminals operating simultaneously and, typically, 6000 baud for a specific demand by a single user.

Hardware Architecture

Each terminal connects to a single USART. Grouped as quads, the USARTs are placed on eight cards, which are all tied to the 8080A system bus (see Fig 2). Two

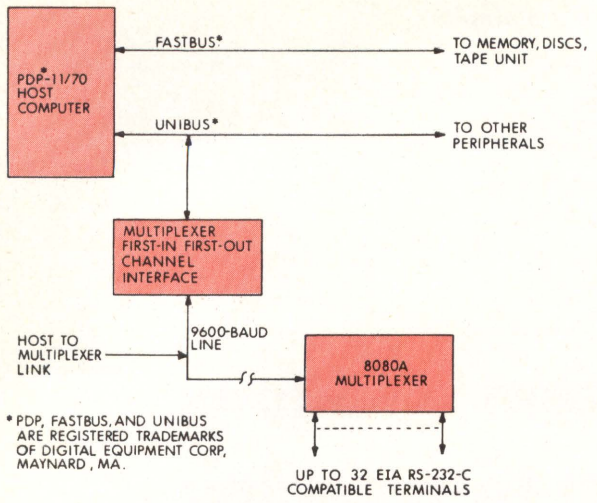


Fig 1 Overall system. Block diagram shows special host computer-to-channel interface: FIFO board and 9600-baud link to 8080A multiplexer. The 32 terminal lines may be any mix of baud rates in groups of four for each rate. Multiplexer may be located in host computer or in its own remote package

8-bit 4k semiconductor random-access memories (RAMs) furnish 8192 bytes of RAM, while 1024 bytes of programmable read-only memory (p/ROM) are available on the microprocessor board. An interrupt controller and a high speed host USART card combine to form a host channel interface board which is also connected to the system bus.

A 128-char buffer is associated with each terminal and USART for output buffering. This buffering takes 4096 bytes of available RAM. The terminal-to-host computer queue is 256 characters long.

Software Routines

The complete software program divides into four routines: (a) the initialize system routine, (b) the polling terminals for I/O routine, (c) the interrupt 1 routine to fill terminal buffers from the host, and (d) the interrupt 2 routine to empty the terminal to host waiting queue (see Fig 3).

Initialization runs only when reset, while the other three routines run in successive order. These routines communicate only through the output data buffers and share no common memory space other than pointer tables. The initialize system routine clears all memory, sets up data tables, determines which boards are plugged in, and resets all USARTs. These tasks comprise approximately all the system housekeeping. In addition, the initialization routine sets the stack pointer, and resets and sets the mode, speed, and number of bits per word on the USARTs.

The polling terminals for I/O routine goes through the list set up by the initialization program and tests to detect whether a character is input, or data are available in a buffer for output. Thus, each of the 32 terminals is serviced once each pass. If the data channel to the host computer is busy, characters are put into a terminal-to-host waiting queue that is serviced when the channel-not-busy interrupt arrives. If the data channel is not busy, the waiting queue, which is set up as a software first-in first-out (FIFO) buffer, is emptied by one character. The channel will then be busy for 1 ms (time interval for one character), and the interrupt will occur again, emptying the queue by one more character. When the queue is empty, the interrupt process will be primed by the clock for data in the queue at the end of every polling loop. Using this technique, the terminal-to-host queue service routine is primed, and continues to be interrupted when not busy, to empty all characters waiting for input into the data channel.

For output data transmission, a tag character for a particular terminal is sent first by the host; then, the character is sent to the host computer via the terminal-to-host queue routine. Each USART board has its own priority table so that only one terminal is processed per pass per board. If a character is transmitted, or if a board has no characters available, the buffer area for each terminal is checked to determine whether an output character is pending. These characters are placed in the buffer by the host-to-terminal service (interrupt 1) routine. When characters are available, the buffer outputs its characters to the USART to be transmitted, and all pointers are updated. When there are no incoming characters, and no output buffer is full, the multiplexer system still polls each USART board for input and each USART buffer for output.

Interrupt 2, the terminal-to-host queue routine, surveys the queue and transmits a character if there is a character waiting; otherwise it returns system control to the polling routine. This queue routine is not called again by an interrupt until the polling routine primes it by sending a character.

The host-to-terminal interrupt routine waits for information to arrive from the host computer before it executes. When a character is received and is ready, an interrupt is generated that starts the interrupt process. This process checks the incoming character and, if it is data, places it in the appropriate output buffer area. After this process is completed, the polling routine resumes. Other characters from the host computer perform status requests, data tag switches, and soft restart commands. The host-to-terminal interrupt routine may interrupt at any time during polling. It first saves the status vector of the machine and then picks up the character that caused the interrupt. If its most significant bit is a 1, the character is a tag or a command (see "Tag/Data and Other Byte Commands"). If it is a tag, it is stored so that the following data characters are loaded into the buffer pointed to by the last tag.

With a most significant bit of 1, the character could also be a command. Commands allowed are: status request, status change, and soft restart. Status request sends back a status tag followed by the status of that USART. Status change takes the next character and transfers it to the USART control register. This can be

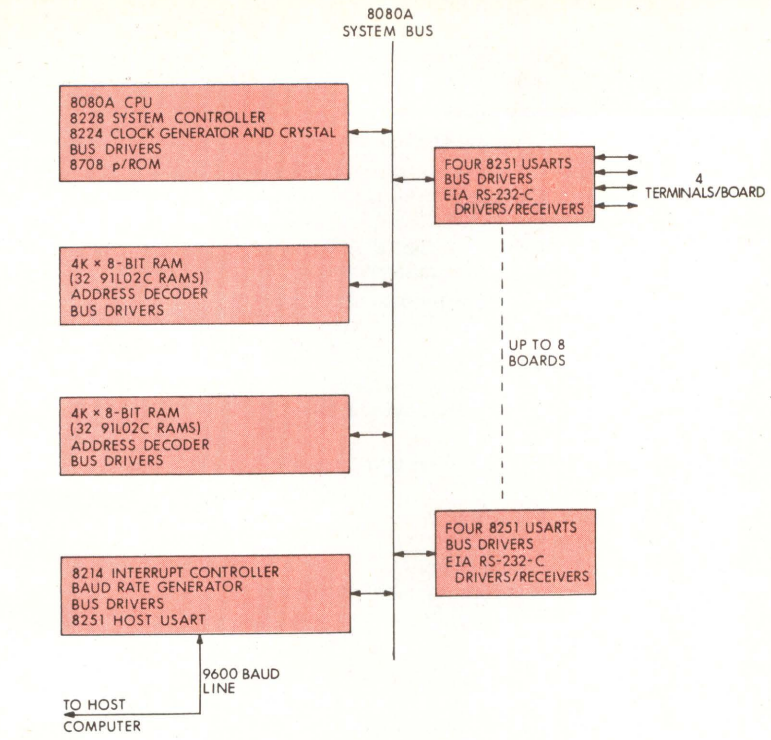


Fig 2 Internal architecture. CPU chip and memory for program are connected to other boards by simple bus system. USART, memory, and host channel interface boards can all be physically connected anywhere on bus. Program determines which USART boards are present before polling so that boards may be removed for maintenance without disabling entire system

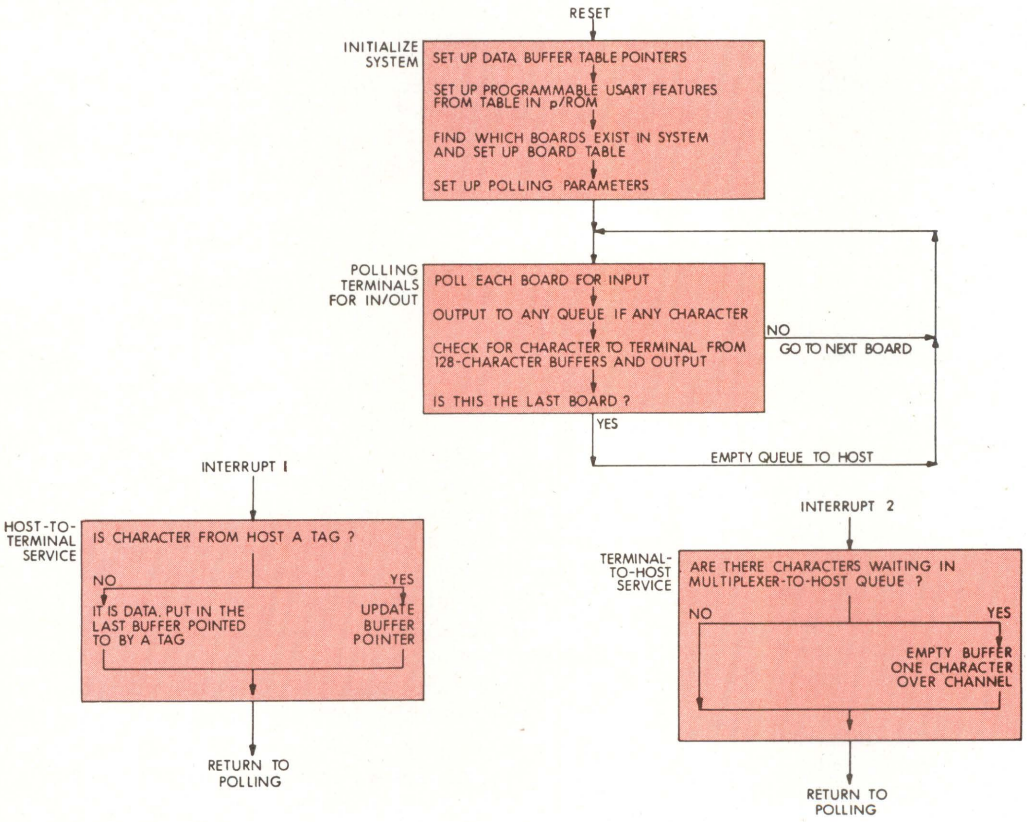


Fig 3 System software. In addition to initialization routine, software has three simple processes: polling USARTs for input characters from terminals, host interrupt with character or tag, and terminal waiting queue to host service interrupt routine. Interrupts are enabled and disabled only so that the tag-data sequence is never violated; otherwise, interrupts may interrupt any routine

used to turn ports on or off, and to change the baud rate by a factor of four for data recording. A 300-baud hardcopy device or a 1200-baud cathode-ray tube (CRT) terminal can be driven by a single line with proper host control. Soft restart re-initializes the entire system. Caution is advised in the use of these controls, since the data buffers will be affected by their use. A speed change could disable interrupts and exceed available polling time, thereby reducing the data rate and possibly causing characters to be lost.

When the most significant bit is a 0, the character denotes data. This character is then loaded into the

Tag/Data and Other Byte Commands

Host Initiated Commands

1000 0000 Restart system

101. .... Send next byte to . .... terminal buffer
(most significant bit must be 0, 7-bit ASCII for the rest of the byte, no parity)

110. .... Send next byte to . .... USART control register

0 ir 0 er 0 Rxe 0 Txe Control byte definition
| if 1 resets USART to "mode"
| reset error flags
| turn on receiver—1, turn off—0
| turn on /off transmitter

0 1 0 0 1 1 1 0 Mode byte for University of California system

111. .... Read data from . .... USART status register
(single byte command, will generate the same command tag followed by the status byte to be returned to the host)

0 0 fe oe pe Txe Rxr Txr Returned byte
| framing error
| overflow error
| parity error
| transmit buffer empty
| receiver ready with character
| transmitter ready

Multiplexer to Host Commands

101. .... Following byte is data from terminal . ....

110. .... Buffer for terminal . ..... is full, no second character sent

This data protocol is used on 8-bit RS-232-C 9600-baud multiplexer. Eight bits are used for both tags and 7-bit ASCII data. Note that eighth bit determines whether byte is tag or data. For data, remaining seven bits are straightforward ASCII. For a tag, further decoding is performed to determine what kind of tag and for what terminal

last place in the buffer pointed to by the tag. All following characters are loaded into the same buffer until a new tag is sent.

Hardware Construction

In addition to the CPU chip and 1k byte of local p/ROM, the multiplexer board contains other support circuits, such as bus buffers, clock drivers, and the crystal-controlled clock. The software program for the multiplexer resides in three p/ROMs on this board.

Two memory boards have 4k 8-bit bytes of storage, using 1k static memory chips, and address selection and bus driver logic.

Designed to perform as a serial data channel with interrupt vector 1, the host channel interface board also has available the other six interrupt vectors and a baud rate generator for the USART; in addition, the board includes vector generator and bus driver. Interrupt vectors and their functions may be summarized as:

Restart (RST) 0: Hardware reset on power-up

RST 1 : Host to multiplexer service routine

RST 2 : Software reset; initializes system and zeros all data buffers

RST 3 to RST 6 : Not used

RST 7 : Channel not busy interrupt from transmit buffer empty on channel USART

Each USART board contains four USARTs, a baud rate generator, and a p/ROM with a priority look-up table. USARTs are addressed as memory locations, as is the p/ROM. Data-available flags of the USARTs, through the p/ROM, place a code on the p/ROM outputs that is the address of the data buffer on the USART that is full. Up to eight of these boards can be utilized in the multiplexer system to accommodate 32 terminals.

The complete multiplexer system contains twelve 4.5 x 6.5" (11.4 x 16.5 cm) printed circuit cards installed in a 20-slot backplane. Including power supplies and a fan, the system occupies a package 9 x 21 x 13" (22 x 53 x 33 cm) and weighs 30 lb (13.5 kg).

Special Host Machine Interface

Because of the load imposed by the multiplexer, a FIFO buffered serial interface board has been designed so that the host computer can transfer more than one character at a time to the internal software buffers. This interface board also prevents a character from being lost by allowing a 32-char buffer to become

half full before the host computer services the data channel. Since the host effects 1 x 10^6 transfers/s, all other higher priority interrupts are serviced first by allowing 16 characters to fill before servicing the interrupt from the host channel. In this case, software overhead is the determining factor in the interrupt service speed.

Located on this board are a host USART, baud rate clock, FIFO buffer chip, and the necessary bus driver logic for operation. The USART performs serial-to-parallel conversion for both transmit and receive. For transmission, data are passed to the USART via bus receivers, and the USART is strobed by the presence of the desired address and timing signals on the control and address section of the bus.

For receive, USART data automatically ripple through the FIFO channel interface until they reach the bus drivers. If there are data in the FIFO buffer, an interrupt is generated. Each time a read is performed in the FIFO buffer, data ripple down one more level if the read has occurred since the last interrupt. In this manner, up to 32 characters are buffered before any can be lost. If host software cannot keep up with the data rate, the FIFO buffer will overflow and data will be lost. An error bit in the status word for this interface board flags the system when overflow occurs. These errors are logged for later investigation.

Clock control is provided by a crystal and divider chain, and all bus logic is supplied by a general-purpose interface card.

System Performance

Channel-to-host data transfer rate is set at 9600 baud for both directions. Characters from each terminal must be echoed as this is a full-duplex system; thus, for every character generated, the host computer must process and return the character to the terminal. In a typical multiplexer system, 20 data entry terminals are set for 9600-baud output and 300-baud input. Also, eight ASR-33 Teletype terminals and four 300-baud dial-up lines are tied to the multiplexer system. For future systems, CRT terminals could easily be substituted for teletypewriters.

An added system feature is that software determines which boards are installed. Therefore a defective board may be removed without affecting the software programming. The same routines, upon re-initialization, will automatically exclude the missing board. In addition, smaller systems may use the same software to perform faster polling for increased input rates, such as with machine-to-machine links.

Typically, the average input rate is 10 char/s, while the average output rate is 200 char/s. Buffers in the host computer that hold characters waiting for an output channel are empty 95% of the time, indicating that the host computer can process data as fast as the channel can handle them, rather than as fast as the terminals can print. Maximum rates experienced are 15 char/s on input, and 620 char/s on output. Maximum and typical figures were obtained with 90% of the terminals on the multiplexer system in use.

Error rates are entirely due to the data channel, or are at least indistinguishable from other errors, such as those caused by operator or host. The host computer, upon encountering a bad disc track, prints a hard error on the system console, forcing a 300-ms deadtime during which no processing is done. Error analysis also has to take into account the number of system messages.

Thus, a data channel is using 1% of the available bandwidth on input, and 20% on output. Recently accumulated data confirm these statistics.

Summary

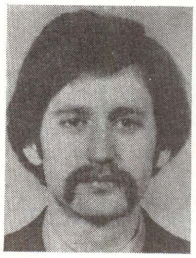
At a cost that is one-fourth that of commercially available equipment, the multiplexer system design described solves many of the communication problems normally encountered in a small timesharing facility. Based on a commercial cost of $300 per terminal, 32 terminals would cost $9600. The multiplexer system design replaces existing hardware and wiring at a cost of less than $2500.

Based on three operational multiplexer systems, accumulated statistics reveal definite system repeatability and reliability. Up time has been better than 95%, exceeding that of the host. Problems to date have been related to connector failures and initial software errors. Future system modifications can easily be made in such areas as: modem control synchronous data links, packet preparation, channel bandwidth maximizing in shared link concentrator systems, and local editing features. Newly incorporated features, such as speed control and character buffering have improved host throughput by 5% and have allowed more flexible usage of a dedicated line. Multiprocessor systems could be used to split input, output, and channel maintenance tasks into separate real-time processes that would increase performance while not substantially increasing costs.

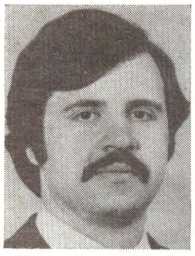
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Microcomputer System User's Manual, Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051, 1975



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Nishan Urkumyan is a development engineer in the support group for digital teaching laboratories at the College of Electrical Engineering and Computer Sciences at Berkeley. He holds a BS degree in electrical engineering from the University of California at Berkeley.

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Electronic Diet Controller

Karen M. Moran

Broomfield, Colorado

One solution to the need for precise regulation of caloric intake, whether for weight gain or loss or other medical reasons, is an electronic controller which tabulates diet information for up to three people, and serves as an all-purpose calculator as well

The cost-effectiveness of microprocessing power now enables solving the problems of controlling principal diet elements with an application that can potentially reach a huge marketplace. As far as is known, the existing method of dietary regulation consists of the haphazard and impractical paper and pencil approach. One additional factor which now makes this application possible is diet lists that are classified into approximately seven food types (meats, fruits, starches, etc) with serving sizes in each food group designed to equal the same number of calories. (These lists are commonly given out by doctors and include a complete tabulation of foods.) As an illustration, the following section is excerpted from the diet list which is published by Carnation Co:

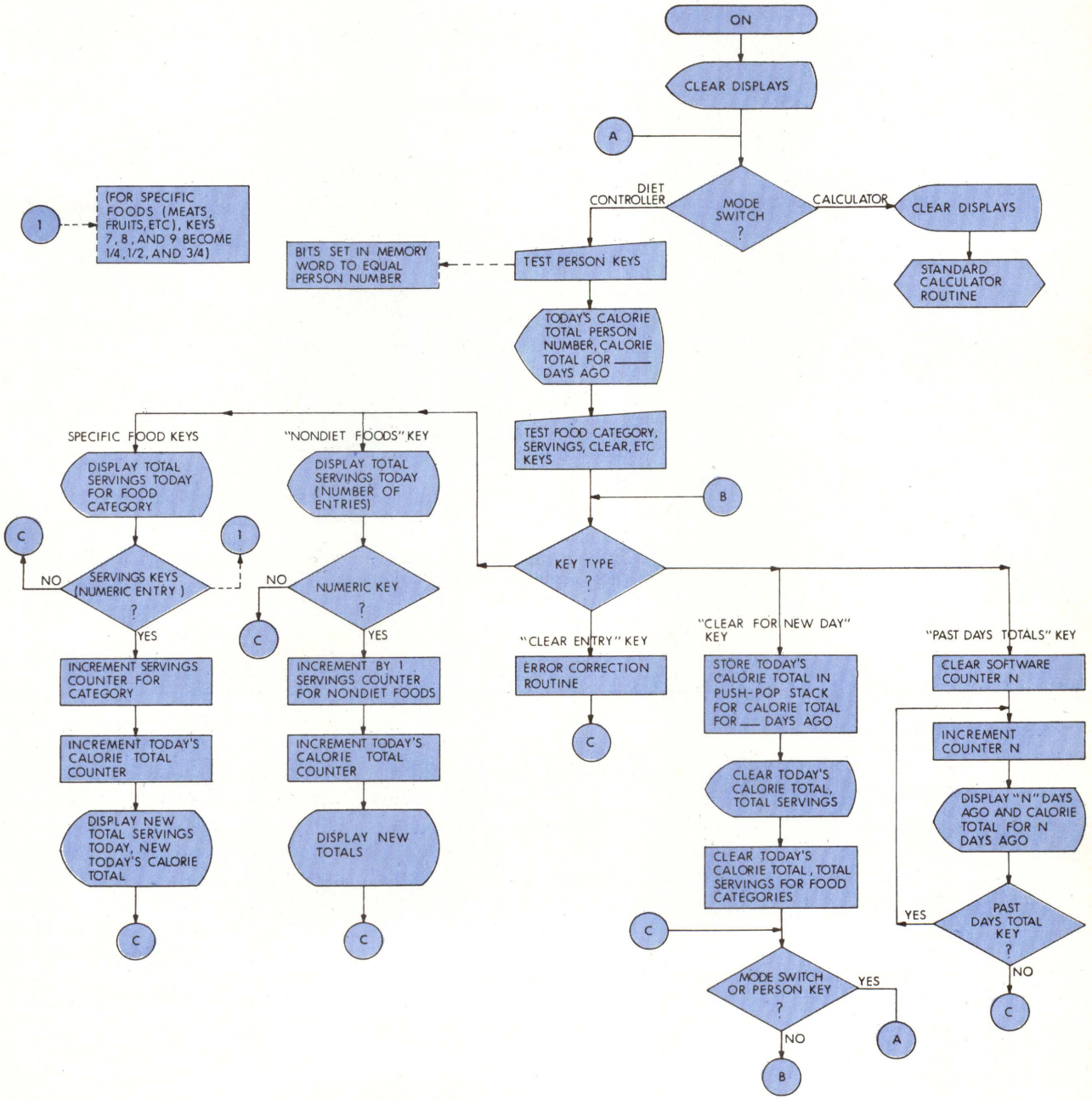
LIST 6 FATS (approx 45 calories/ amount indicated)

Avocado (4" diam)—⅛
Bacon, crisp—1 slice
Butter, margarine—1 tsp
Cream, sour—2 T
Cream cheese—1 T
Nuts—6 small
Dressing, French—1 T
Mayonnaise—1 tsp
Roquefort dressing—2 tsp
1000 Island dressing—2 tsp
Oil—1 tsp
Olives—5 small

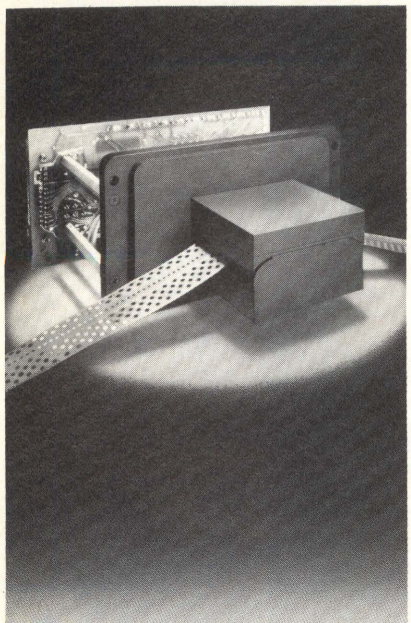
For occasional reference, a diet list in this same format, along with a non-diet food list (containing caloric values) would accompany the controller. This information could be available either at the back of the device or along with the instruction pamphlet.

In actual operation (see the Figure), the user, for example after having one frankfurter, one hot dog bun, half an apple, and a glass of milk for lunch, keys in: person 1, meat 1, starch 2, fruit 1, and milk 1. Meanwhile, the controller, by doing a simple table lookup for the calorie values, is concurrently updating and displaying "Today's Calorie Total" and "Food Category: Total Servings Today." Hence, the user enters the serving number and is able to read the new calorie and serving totals on the displays. (Since many diets require a

Flowchart


ON
CLEAR DISPLAYS
A
MODE SWITCH ?
DIET CONTROLLER
CALCULATOR
CLEAR DISPLAYS
STANDARD CALCULATOR ROUTINE
1
(FOR SPECIFIC FOODS (MEATS, FRUITS, ETC), KEYS 7, 8, AND 9 BECOME 1/4, 1/2, AND 3/4)
BITS SET IN MEMORY WORD TO EQUAL PERSON NUMBER
TEST PERSON KEYS
TODAY'S CALORIE TOTAL PERSON NUMBER, CALORIE TOTAL FOR ___ DAYS AGO
TEST FOOD CATEGORY, SERVINGS, CLEAR, ETC KEYS
B
KEY TYPE ?
SPECIFIC FOOD KEYS
"NONDIET FOODS" KEY
"CLEAR ENTRY" KEY
"CLEAR FOR NEW DAY" KEY
"PAST DAYS TOTALS" KEY
DISPLAY TOTAL SERVINGS TODAY FOR FOOD CATEGORY
DISPLAY TOTAL SERVINGS TODAY (NUMBER OF ENTRIES)
C
1
SERVINGS KEYS (NUMERIC ENTRY) ?
NO
YES
NUMERIC KEY ?
NO
YES
INCREMENT SERVINGS COUNTER FOR CATEGORY
INCREMENT BY 1 SERVINGS COUNTER FOR NONDIET FOODS
INCREMENT TODAY'S CALORIE TOTAL COUNTER
INCREMENT TODAY'S CALORIE TOTAL COUNTER
DISPLAY NEW TOTAL SERVINGS TODAY, NEW TODAY'S CALORIE TOTAL
DISPLAY NEW TOTALS
ERROR CORRECTION ROUTINE
STORE TODAY'S CALORIE TOTAL IN PUSH-POP STACK FOR CALORIE TOTAL FOR ___ DAYS AGO
CLEAR TODAY'S CALORIE TOTAL, TOTAL SERVINGS
CLEAR TODAY'S CALORIE TOTAL, TOTAL SERVINGS FOR FOOD CATEGORIES
MODE SWITCH OR PERSON KEY ?
YES
NO
A
B
CLEAR SOFTWARE COUNTER N
INCREMENT COUNTER N
DISPLAY "N" DAYS AGO AND CALORIE TOTAL FOR N DAYS AGO
PAST DAYS TOTAL KEY ?
YES
NO

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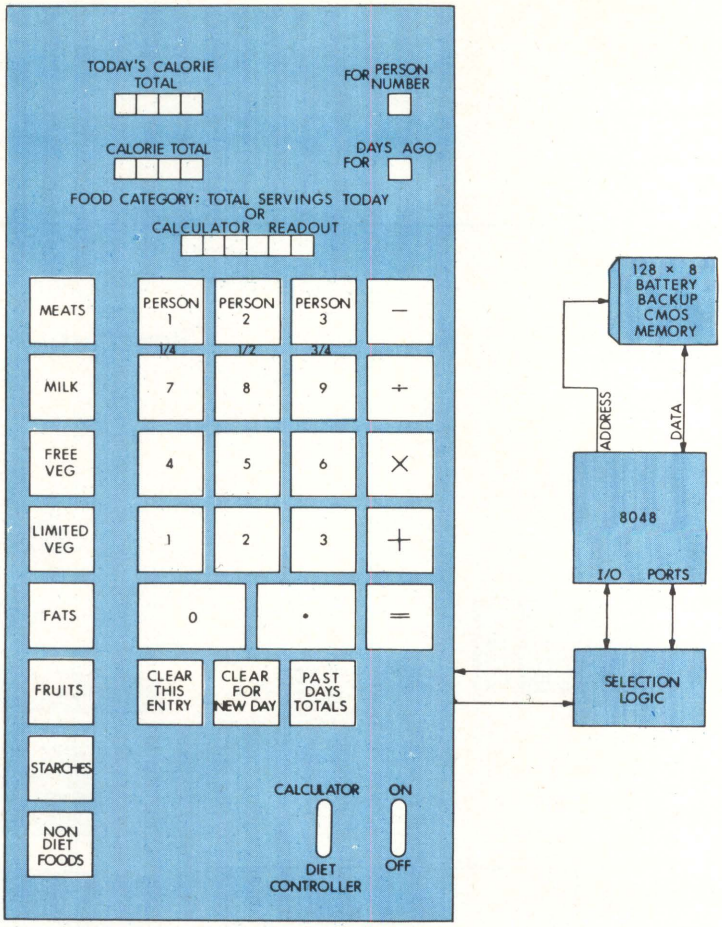
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Keyboard design of microprocessor-based controller contains keys necessary to govern diet by accounting for all foods and keeping track of daily and accumulated calorie totals for up to three people. Complete with an 8048 microprocessor and 128 x 8 CMOS memory, device can also be utilized as a calculator

certain number of servings in the various food categories, this history information is available by depressing the appropriate food category key.) If the user also had a piece of chocolate cake, he keys: nondiet food, 445 (actual number of calories). The controller, in addition, keeps track of calorie totals for the past six days, and also allows for three users. In short, it provides the necessary information for making food selection judgments throughout the day. (For complete details on the operation of the device, including clearing for a new day and error correct, see the program Flowchart.)

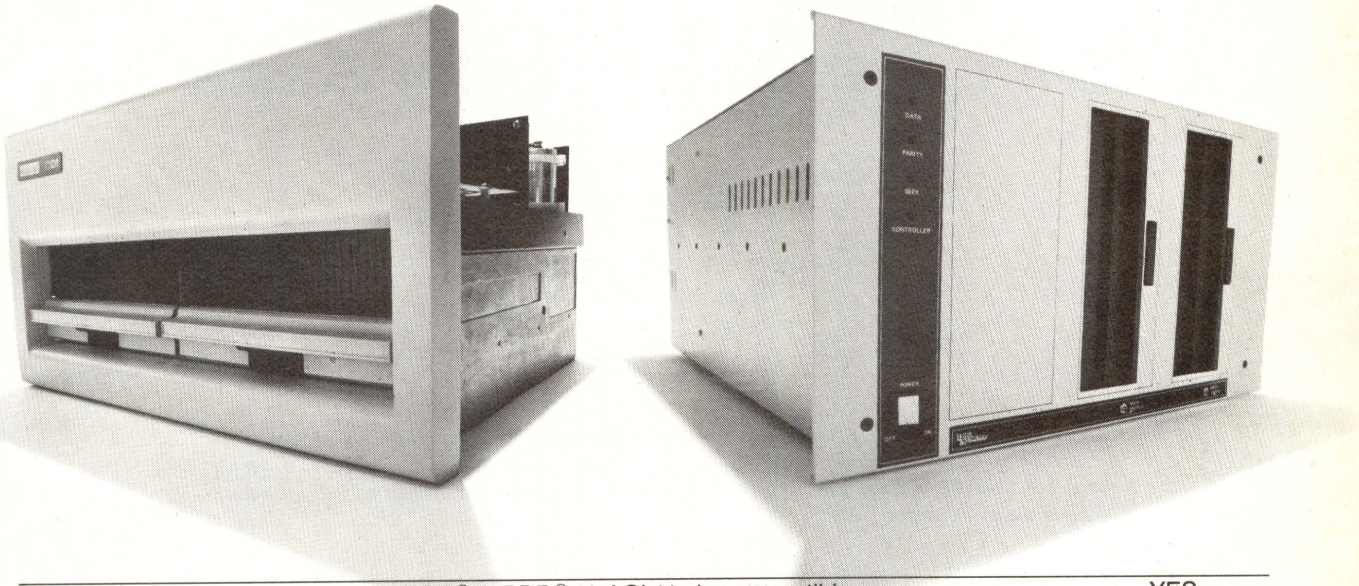
This system can, of course, be used by those who need to gain weight, or it can be adapted for special diets. Note also that since all the hardware is already present, the controller can be used as a calculator—perfect for kitchen use as an aid to multiplying and dividing recipes, balancing the checkbook, etc.

System elements include an Intel 8048, an additional 128 x 8 CMOS memory with battery backup, selection logic, keyboard, and displays. Hardware and software aspects of this application represent a completely practical use of today's technology; no problem areas are foreseen. □

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NO	Write protect switches	**YES**
YES	Automatic head unload	YES
YES	Ceramic read/write head	YES
YES	Holds 256,256 bytes per diskette	YES
NO	Diskette formatting capability	**YES**
1 OR 2	Drives per controller	**1, 2, OR 3**
NO	Interchangeable 50/60 Hz operation	**YES**
YES	Digital phase-lock-loop data separation circuit	YES
NO	Front panel activity LED lights	**YES**
NO	Front panel system status indicators	**YES**
PARTIAL	Modular construction	**COMPLETE**
MINIMAL	Self-testing microcode	**EXTENSIVE**
NO	Field-proven Shugart drives	**YES**

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CIRCLE 62 ON INQUIRY CARD

DESIGN NOTE

An Asynchronous Arbiter Resolves Resource Allocation Conflicts On a Random Priority Basis

K. Søe Højberg

Research Establishment RISØ
Roskilde, Denmark

When two or more processors demand service from a shared bus in an asynchronous mode, conflict resolution and resource allocation are solved fairly by an arbiter system that scans and selects processors at random, independent of time of request

Conflicts may occur when two or more devices in a parallel system share a functional resource and request it on an asynchronous basis. To decide these conflicts and to allocate the shared resource equitably, an arbiter is required. A typical system necessitating an arbiter is a multiprocessor with one common bus; the arbiter is used to resolve overlapping bus transaction requests. Pierce,[1] et al, described a simple 2-input arbiter circuit that can be used as a module in an n-input arbiter tree. The fraction of service given to a requesting device depends on the position of the corresponding arbiter module in the tree structure. Plummer,[2] et al, described a rather general but more complicated system.

This relatively simple arbiter system is a supplement to both references. It does not have a tree structure but it does include a set of parallel request/grant channels. The fraction of service given is identical for all arbiter channels.

Signaling Conventions

The block diagram of a multichannel arbiter is shown in Fig 1(a); signaling conventions are illustrated in Fig 1(b). A device requests the shared resource by raising its request line R_j, where $j = 1 \ldots n$. Requests are initiated by a device only when its grant line G_j is low. The arbiter allocates the shared resource to a particular device, say number j, by raising its grant line G_j. When the requesting device j finishes using the resource, it resets its request line R_j, which causes the arbiter to reset the corresponding grant line G_j.

Arbiter Operation

Fig 2 illustrates the multichannel arbiter system. The clear inputs of the flip-flops must be of the direct type. Thus, any true clear input, CLR_j, resets its associated output, G_j, immediately when applied. A dual-phase clock is assumed. Time between succeeding pulses can be increased arbitrarily. This means that pulses can be triggered by pushbutton control as well as by a square-wave generator. In the latter case, for example, clock 1 impulses can be released by the leading edge, and clock 2 impulses by the trailing edge of the signal.

Fig 3(a) shows waveforms associated with the single-request case. Initially, all requests and grants are assumed to be zero. A single request, R_j, passes through the system (Fig 2) in a direct manner and produces a

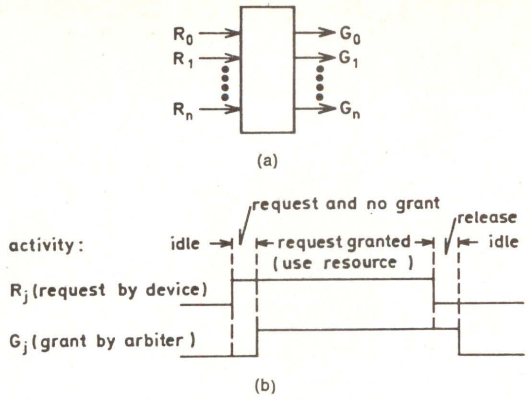


Fig 1 N-channel arbiter resolves conflicts when several devices simultaneously request a shared resource. In (a), $R_0 \ldots R_n$ are request lines; $G_0 \ldots G_n$ are grant lines connected to devices 0, 1 . . . n. In (b), requests are initiated by device upon issuing a ONE signal at its request line. Arbiter allocates resource to device by answering with a ONE signal at corresponding grant line. At a given time, not more than one grant is true

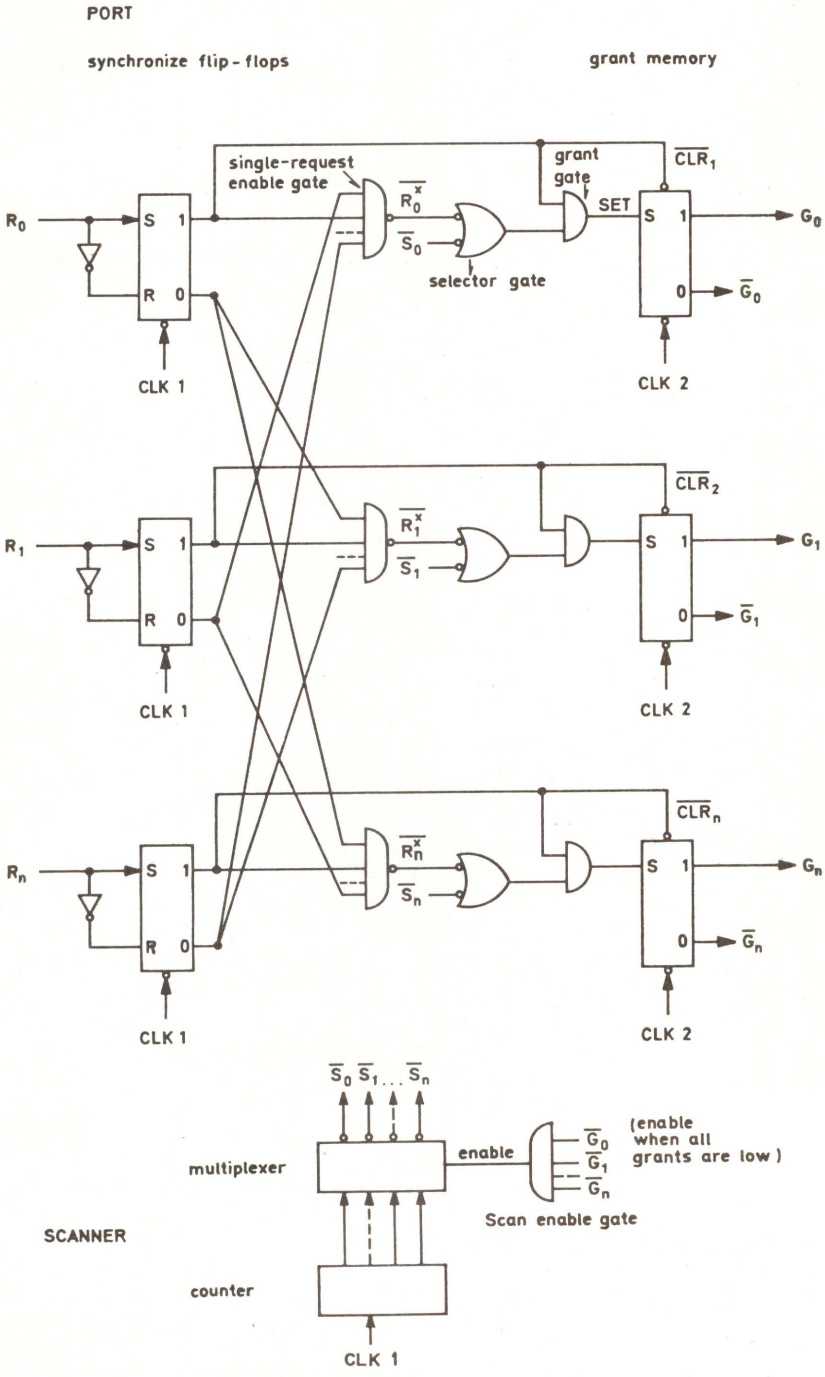


Fig 2 Multichannel arbiter system. Single requests pass through channel and release grant in a direct manner. Multirequest conflict is resolved by scanner that selects channels one at a time. When true scanner output, S_k ($k = 1 \ldots n$), coincides with true request signal R, grant G_k is issued. Irregular request frequency is assumed; at regular frequencies with possible interaction with clock frequency, scanner should be replaced by random number generator

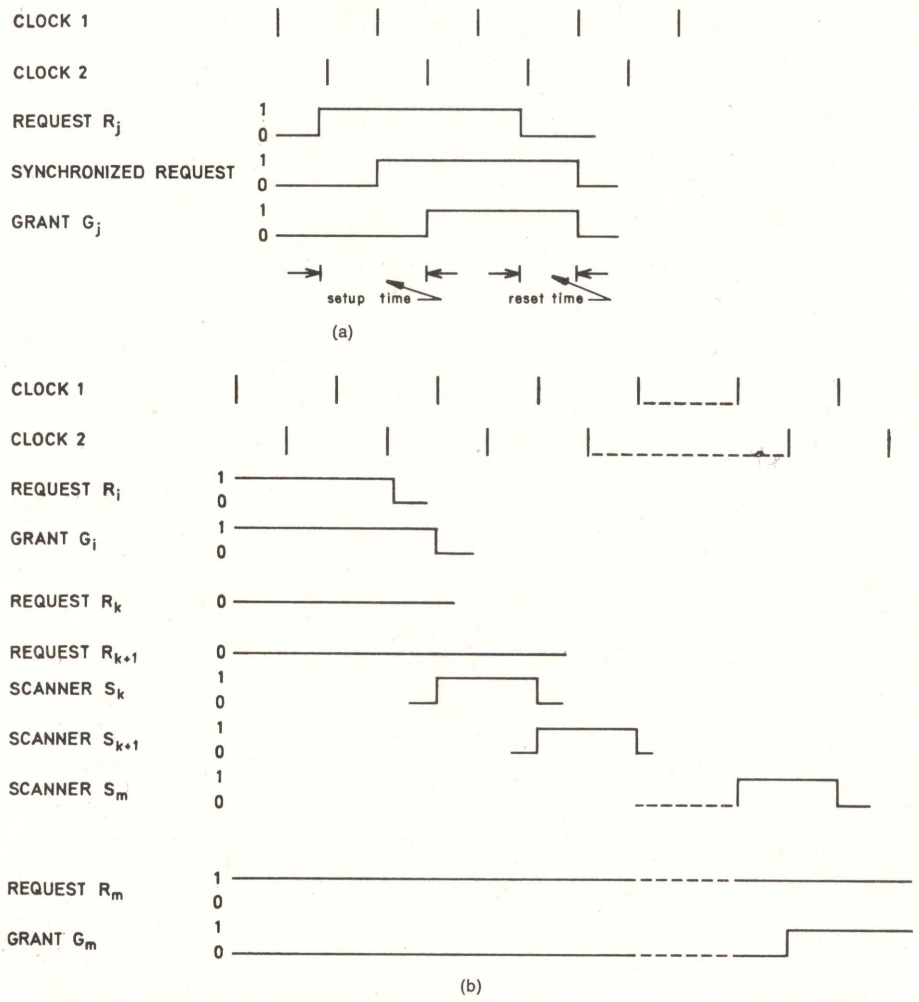


Fig 3 Three cases of arbiter operation. Single-request response (a) needs only a 0.5 to 1.5 clock cycle to set up a grant, depending on time of request. In medium-load case (b) at least three requests initially are present. When request R_i and corresponding grant G_i disappear, request lines are scanned and an arbitrary channel with ONE input is selected. Number of scanning steps used depends on start position of scanner. In full-load case (c), only 0.5 clock cycle is used from the time when one grant has disappeared until another grant is issued

grant, G_j. The synchronized request signal passes through the enable gate and selector gate, as enable signals are present from all other request flip-flops (inverted synchronized requests are true). The selector gate includes an OR circuit, as shown in Fig 2, for selection of a single request, such as R_o^x or a scan output signal S_o. The OR output passes through the grant gate and sets the grant flip-flop. The grant gate functions as an AND gate for scanner signals and does not hinder single-request signals. In this manner a scanner signal can only set a grant if a request is present in the given channel.

The request arrival to grant setup time corresponds to a 0.5 to 1.5 clock cycle, as indicated in Fig 3(a). Fig 3(b) illustrates the medium-load case. Requests R_k and R_{k+1} are not present. Request R_i and at least two more requests, including R_m, are present so that all direct paths are inhibited when R_i disappears. In this case the scanner is exploited for grant setup. The multiplexer is enabled by the disappearing grant. The first true scanner output happens to be S_k, which is not gated to the grant flip-flop. The scanner moves one step to channel k+1, which also does not create a grant. At the first channel to be met with a true request input, say channel m, a grant is produced.

Note that the counter runs continuously. If the time duration between multiplexer selections is random, the channel numbers chosen are random. This duration is determined by request periods and the delay caused by the arbiter. Another method of obtaining randomness of channel selection is by changing the clock pulse duration at random. Still another method is to use an alternative scanner that includes a random number generator.

Fig 3(c) illustrates the full-load case. All request inputs are true. Only grant G_j is true. When request R_j is changed from true to false, grant G_j disappears within one clock period. The multiplexer is enabled, and if the output S_i at channel number 1 happens to be true, grant G_i is issued with a delay of only a 0.5 clock period. Concerning the randomness of channel selection, the considerations are similar to those given for the medium-load case.

System Verification Test

A 3-channel arbiter circuit was implemented with high speed TTL components including master-slave flip-flops. A square-wave clock generator controlled two monostable impulse generators for clock 1 and clock 2 realization. Impulse widths were 30 ns. The frequency of the basic clock was varied from zero to the maximum applicable frequency. With simultaneous requests applied, only one grant at a time was obtained in the range up to 15 MHz; extra grants were often issued above 15 MHz. The delays of the TTL circuits involved indicate a reasonable working frequency for the test circuit to be 10 MHz, corresponding to a clock period time of 100 ns.

A special test was implemented with an inverted channel output $\overline{G}_o$ connected to channel input R_o. (See Fig 2). Other request inputs were kept at zero. In this case a request was automatically generated when the grant was false, and the request disappeared when the grant became true. Thus, the system worked automatically at maximum speed using all the time for administrating and producing its own inputs. Total cycle time for setting up a grant, resetting the grant, and producing a request was 200 ns at a 10-MHz clock frequency.

Summary

This relatively simple high speed multichannel arbiter serves as a supplement to earlier designed systems (Refs 1 and 2). Load properties are optimal both at full-load and single-request conditions.

Acknowledgement

Thanks are due to J. R. Taylor and J. V. Olsen for valuable discussions leading to system improvement.

References

1. W. W. Plummer, "Asynchronous Arbiters," *IEEE Transactions on Computers*, Jan 1972, pp 37-42
2. R. C. Pearce, J. A. Field, and W. D. Little, "Asynchronous Arbiter Module," *IEEE Transactions on Computers*, Sept 1975, pp 931-932

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CIRCLE 63 ON INQUIRY CARD

Microcomputer Interfacing: Interfacing Analog-to-Digital Converters

David G. Larsen
Peter R. Rony
Virginia Polytechnic Institute & State University

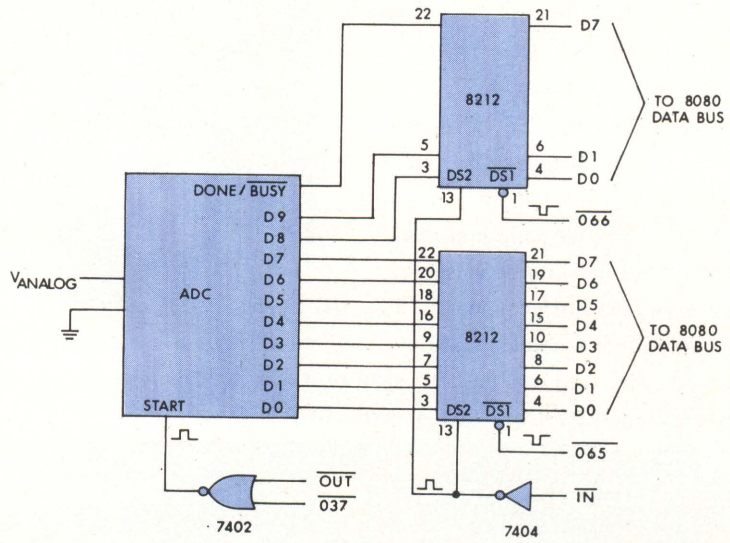
Christopher Titus
Jonathan A. Titus
Tychon, Inc

Typical commercial analog-to-digital converters (ADCs) are based upon the principles of successive approximation, dual-slope integration, staircase-ramp conversion, or voltage-to-frequency conversion.* The most common use for an ADC is to convert output from an analog transducer or analog instrument into digital form suitable for direct observation on a digital display or as input into a computer. All digital panel meters and digital multimeters contain built-in ADCs. Modern ADCs provide standard TTL outputs which may be coded in binary, binary-coded decimal (BCD), or perhaps other less frequently used codes.

To illustrate the interfacing of an ADC to an 8080-based microcomputer, consider the generalized 10-bit ADC module shown in the Figure. In addition to 10-bit output and analog input pins, the module also contains a START input and a DONE/$\overline{\text{BUSY}}$ output whose functions will be discussed later. As previously observed from the discussion on interfacing of a 10-bit digital-to-analog converter (DAC) in the "Micro Processor/Computer Data Stack," *Computer Design*, June 1977, pp 203-205, it is not possible to simultaneously transfer all ten bits from the ADC into an 8-bit microcomputer. For the 10-bit converter, data transfer is accomplished by placing bits D0 through D7 [the ADC's eight least significant bits (LSB)] in the first input byte and the remaining two bits, D8 and D9 [the ADC's most significant bits (MSB)], in the second byte.

To gate data onto the data bus and into the 8080, 8212 8-bit, 3-state buffer chips are used between the converter's outputs and the 8080 data bus. A gating scheme is required so that the 3-state buffers are enabled only when the 8080 requests data. In the case of the 8212 buffer, the required gate is incorporated within the integrated circuit chip, so all that is needed is a negative $\overline{\text{IN}}$ control signal, and negative 065 and 066 decoded pulses derived from the address bus decoding logic.

**Analog-Digital Conversion Handbook*, Analog Devices, Inc, Norwood, Mass (Copies cost $3.95)



Schematic diagram of ADC interfaced to 8080 microcomputer with the aid of a pair of 8212 buffer chips

TABLE 1

Typical Input Routine for a 10-Bit ADC

```
                          *100  000
100  000  365   ADC,      PUSHPSW     /Save register A & flags
100  001  323             OUT         /Strobe the ADC to start a conversion
100  002  037             037
100  003  333   TEST,     IN          /Input status bit and two MSBs
100  004  066             066
100  005  306             ADI         /Add 1 to the flag bit
100  006  001             001         /to cause a carry if it is set
100  007  322             JNC         /No overflow, check it again
100  010  003             TEST
100  011  100             0
100  012  107             MOVBA       /Overflow, flag = 1, so save MSBs
100  013  333             IN          /Input the eight LSBs
100  014  065             065
100  015  117             MOVCA       /Store them in register C
100  016  361             POPPSW      /Restore register A & flags
100  017  311             RET         Return to main program
```

TABLE 2

Typical ADC Subroutine for an Interrupt-Type Converter Interface

```
                          *100  000
100  000  373   ADC,      EI          /Enable the 8080's interrupt
100  001  323             OUT         /Start a conversion
100  002  037             037
100  003  311             RET         /Return to main program
                          This is the ADC's interrupt service software
                          *000  070
000  070  365   ADCSVC,    PUSHPSW     /Save register A & flags
000  071  345             PUSHH       /Save registers H & L
000  072  052             LHLD        /Get memory pointers into H & L
000  073  000             POINT       /so the data may be stored
000  074  120             0
000  075  333             IN          /Input eight LSBs
000  076  065             065
000  077  167             MOVMA       /Store them in memory
000  100  043             INXH        /Increment memory pointer
000  101  333             IN          /Input two MSBs
000  102  066             066
000  103  167             MOVMA       /Store them, too
000  104  043             INXH        /Increment memory pointer again
000  105  042             SHLD        /Save the storage area address
000  106  000             POINT
000  107  120             0
000  110  341             POPH        /Restore registers H & L
000  111  361             POPPSW      /Restore register A & flags
000  112  311             RET         /Return to main program
                          *120  000
120  000  000   POINT,    000         /This is where the address of the ADC
120  001  020             020         /storage area is kept. In this program
                                      /the storage area starts at
                                      /address 020 000. You could place your
                                      /own pointer address here, but these
                                      /two locations must be in R/W memory
```

Note: This subroutine assumes the converter will interrupt with an RST 7 instruction vectoring to 000 070.

Remaining control signals that are used include (1) a START pulse, which when applied to the ADC resets it and starts the internal conversion process, and (2) a DONE/$\overline{\text{BUSY}}$ ADC output flag, which indicates that a conversion has taken place and that the 10-bit digital output is ready. These are important control signals since they synchronize the operation of the conversion process. ADCs generally are not "free-running" devices that continuously convert voltages into digital outputs. These conversions take a finite period of time. It is necessary to pulse or strobe the ADC to start each conversion, and a 10-bit binary value cannot be expected to be output by the converter immediately after the strobe pulse is applied. For the generalized converter in the Figure, a 21-μs conversion time is required. Inside the ADC, a successive approximation technique is used that converges on the unknown voltage by making successively smaller tests and comparing results of such tests to the unknown voltage.

The DONE/$\overline{\text{BUSY}}$ flag, which indicates that the converter is either DONE (logic 1) or $\overline{\text{BUSY}}$ (logic 0), is input to the microcomputer as a single bit. Since there are six unused bits at input port 066, bit D7 is assigned to the flag. The START pulse to initiate a conversion must be a short positive pulse; it can be obtained by gating the control signal $\overline{\text{OUT}}$ with a negative device address pulse, $\overline{037}$, using a 7402 2-input NOR gate.

A typical software subroutine used to perform a single conversion is shown in Table 1.** The 10-bit binary result of the conversion is left in the B and C registers of the 8080, with the eight LSBs in register C and the two MSBs in register B in bit positions D0 and D1. The microcomputer spends time in the TEST loop as it checks and rechecks the flag bit while the conversion takes place. The converter we chose took only 21 μs; so the computer is only dedicated to the loop for a short period.

For other types of converters, the conversion time may take much longer, perhaps milliseconds, or even hundreds of milliseconds for a digital multimeter. In such a case, the microcomputer would spend considerable time waiting for the ADC to "flag" the 8080, indicating that the conversion was complete.

An alternative approach is to use the DONE/$\overline{\text{BUSY}}$ flag as an interrupt input to the 8080. After initiating a conversion by outputting a START pulse, the microcomputer goes to some other software task while the conversion proceeds. When the conversion is complete, the ADC interrupts the computer and points it to the ADC's service software, which in this case is located at 000 070. A software example is provided in Table 2. In this example, the ADC subroutine is used only to start the conversion process. The subroutine at 000 070 is called by the interrupt with the aid of a jammed RST 7 instruction byte. The ADC interrupts the 8080 only when it has finished a conversion. Software starting at 000 070 inputs the ten bits of data and stores them in a data file. As stated previously ("Micro Processor/Computer Data Stack," *Computer Design*, Nov 1976, pp 142-143), interrupts should be used with caution.

**The assembly language format shown in Tables 1 and 2 is that of the resident editor/assembler developed by Tychon, Inc for 8080 systems.

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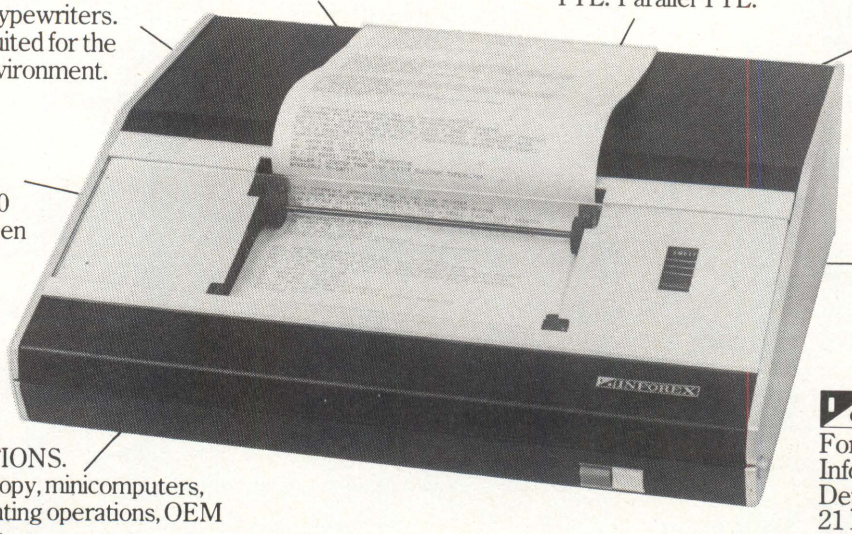
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8-Bit System

An 8-bit device based on the 8080A microprocessor, H8 is a general-purpose computer for the beginning or experienced hobbyist. Intended for expandability and flexible operation, the computer features a built-in 1k x 8 ROM containing a monitor program for controlling the front panel and load-dump operations. The resident monitor has built-in bootstrap for 1-button program loading or storing. The cabinet is configured for 32k of memory with a total capacity of 65k of addressable memory.

An intelligent front panel with 9-digit, 7-segment octal display and keyboard allows greater user control. Register and memory contents can be displayed dynamically while programs are running.

Additional features include a 16-digit keyboard, built-in programmable speaker, and LED status lights. Bus design is a 10-slot motherboard utilizing 50-pin connectors for expansion capability. Convection-cooled power supply handles up to 32k of memory and two I/O interfaces.

Mail order price of $375 includes a fully wired and tested CPU, assembly and operations documentation, and systems software in audio cassette form. Accessories include an 8k board with 4k of static RAM ($140), a 4k expansion chip set ($95), serial I/O interface board with 1200-baud audio cassette interface ($110), and 3-port parallel interface ($150).

16-Bit Computer

Utilizing the DEC LSI-11 microcomputer module with the PDP-11 instruction set (see *Computer Design*, "Digital Technology Review," March 1975, pp 16, 18), the H11 features the 16-bit CPU with a 4k x 16 dynamic RAM. Memory is expandable to 20k.

Unit includes built-in backplane, and power supply with switching regulators and full circuit protection. A DEC system software package is also included, containing editor, PAL-11 assembler, linker, online debug package (ODT), I/O executive, BASIC, and FOCAL. Owners are also eligible for DECUS, the DEC user's organization.

Digital Equipment Corp and Heath have signed a contract for the LSI-11 microcomputers and related products. The agreement includes a licensing arrangement providing use of assembly and higher level programming languages with the H11 computer.

Mail order price of the 16-bit computer is $1295. Accessories include a 4k x 16 static RAM board ($275), flexible serial interface ($95), and parallel interface ($95). The 30-char/s LA36 DECwriter II terminal is offered through Heath for those requiring hardcopy printout.

Computer Peripherals

System-compatible peripherals for the two computers include a CRT terminal, paper tape reader/punch, serial and parallel interfaces, a hard-copy printing terminal, and cassette player/recorder. I/O interfaces, additional memory, and supplementary software packages complete the initial product offerings.



Peripherals, compatible with the two Heath computers as well as others, include the H9 12" (30.48-cm) CRT terminal with 67-key ASCII keyboard and 5 x 7 dot matrix display

Designed to accompany the H8 and 11 computers, the H9 alphanumeric video terminal will work with any digital computer. It utilizes a 67-key ASCII keyboard with 12-line, 80-char format on a 12" (30.48-cm) CRT. Other features include a format option of 12 lines, 20 char wide; cursor control; batch transmit feature; and plot mode. Standard serial interfaces include EIA 20-mA loop, and TTL I/O; baud rate is selectable from 110 to 9600. Price is $530.

The H10 paper tape reader/punch is a mass storage peripheral unit that also functions with other digital computers. Using a standard 1" (2.54-cm) wide roll or fan-fold 8-level paper tape, the reader reads tape at 50 char/s while the punch operates at 10 char/s. Punch and reader circuits are independent; they may be operated simultaneously. Features of the $350 unit include copy mode for tape duplication, built-in heavy duty power supply, and stepper motor for reliable reader tape drive. Interface is standard parallel TTL.

Shipments of all these computer products are scheduled for the fall. Systems are backed by complete documentation and service support, self-instructional . programming courses, and a Heath User's Group (HUG).

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Using the 8080A microprocessor, the Heath H8 is part of a line of hobby, home, educational, and small business computer kits. Computer features an intelligent front panel with octal data entry keyboard and 9-digit, 7-segment display

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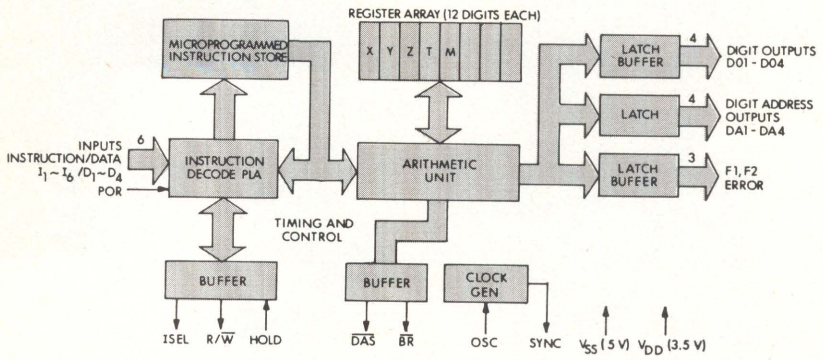
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processor is a single-chip arithmetic unit (calculator) designed to perform complex number processing operations. It interfaces to either a microprocessor-driven or random-logic system.

The MM57109 is a preprogrammed microcontroller that combines scientific calculator functions, test and branch capability, internal number storage, and I/O functions on the same chip. National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051 has added the "number cruncher" unit (NCU) to its COPS Controller Oriented Processor Series (See *Computer Design*, "Micro Processor/Computer Data Stack," March 1977, pp 128, 130).

Basically a scientific calculator without a keyboard or display, the unit eliminates most software development chores and peculiarities of data transfer encountered when general-purpose microprocessors are used for these tasks. Major advantage is no software development costs.

The microprocessor easily interfaces with most I/O functions because it has a single clock, low power operation, single 9-V power supply, and separate digit input, output, and address bus. It is TTL-compatible and can be operated from 5- and −4-V power supplies.

The device accepts a series of BCD digits with a single input instruction, an asynchronous digit input, or single-bit input, rather than with data bytes. Chip has a preprogrammed instruction set similar to those of scientific calculators which use Reverse Polish Notation; thus, software necessary for trigonometric, logarithmic, and exponential operations is built directly into the device.

Programming is done in a language similar to calculator keyboard level language with simplified software development and more reliable generated code. Internal data word contains 12 digits, each consisting of four bits. All functions are accurate to eight digits.

When used as a standalone processor in many control applications, the NCU receives instructions from an external source (p/ROM) and program counter in 6-bit form (6-bit opcode). Alternatively, it can be configured as a peripheral device on the bus of a micro or minicomputer system (such as SC/MP) to expand the CPU's power. A full range of interface and support circuits is provided for the device.

Minifloppy Hobby Kit Operates With S-100 Bus System

The Z//25 FORTRAN IV-minifloppy™ kit includes a Shugart SA400 minifloppy disc drive, cables, and cabinet; and interface module kit. Disc operating system (FDOS) with file management; Sysgen program to personalize the system; text editor; and FORT//80, FORTRAN IV for the 8080 microcomputer (see *Computer Design*, "Micro Processor/Computer Data Stack," Nov 1976, p 148) are all contained on a Shugart SA105 minidiskette™. Available from Realistic Controls Corp, 3530 Warrensville Center Rd, Cleveland, OH 44122, the kit operates with any standard S-100 bus system with 20k of RAM.

Interface module is a disc driver and parallel I/O module in one. It features an onboard crystal-controlled timer, providing compatibility with any 8080 series processor, independent of cycle time. The S-100 bus-pluggable, fully socketed PC board also has an onboard bootstrap and diagnostic p/ROM. The interface can control two minifloppy drives. Power is supplied from the S-100 bus, with onboard power regulators for the first drive; power regulation hardware is supplied with the second drive, when ordered.

Vectored interrupts are selectable to any of seven possible vectors with software sensing of interrupt enable/disable status. The module also includes an 8-bit parallel input port with input strobe and an 8-bit parallel latching output port with output strobe.

The kit is priced at $1095; assembled and tested, it is $1220. A second minifloppy drive, regulator, and cable kit sells for $449 ($495 assembled and tested). Additional formatted diskettes are $5.

Circle 171 on Inquiry Card

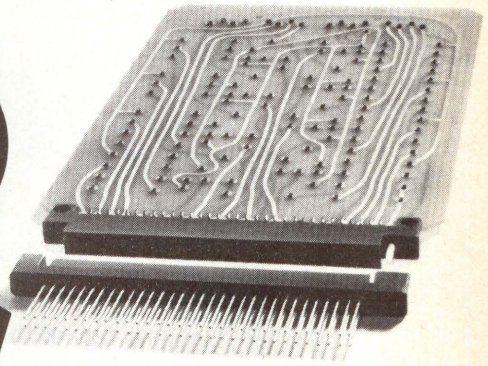
Nonimpact, High Speed Printer Utilizes Electric Discharge Technology

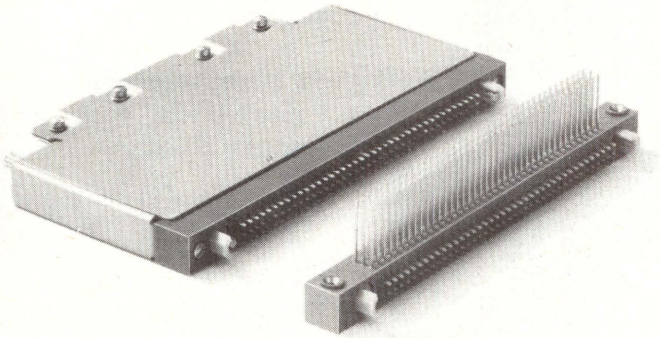
Designed as a nonimpact printing device using electric discharge technology and special aluminum coated paper, the Micro 1 is a high speed, low cost, compact microprinter aimed at microprocessor-oriented markets including home and hobby devices. The 240-char/s printer is offered as a complete unit including case, power supply, 96-char ASCII generator and interface, paper roll holder, infrared low paper detector, bell, and multiline asynchronous input buffer.

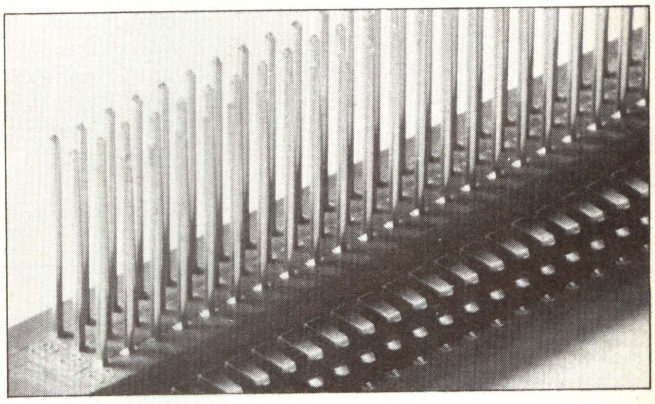
The printer was developed jointly by Centronics Data Computer Corp, Hudson, NH 03051 and Sharp Corp, Osaka, Japan, who have also signed a long term supply-purchase agreement. The printer produces copy on aluminum coated paper by discharging a low voltage electric arc through the styli which melts the coating (less than 1 micron thick), exposing the black background. Toners and ribbons are not required.

(Continued on p 132)

How to get a lot more into a lot less.







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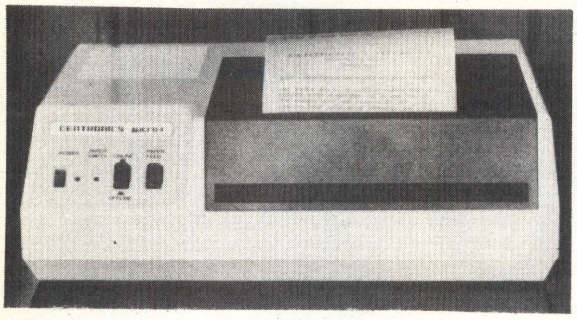
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CIRCLE 67 ON INQUIRY CARD



High speed, low cost, compact microprinter from Centronics features electrosensitive printing at 180 lines/min on aluminum-coated paper, eliminating ribbons, toners, and sensitivity to light, heat, and humidity

The elongated 5 x 8 dot matrix printed characters, unlike those resulting from thermal printing, are impervious to light, temperature, and humidity. In addition, the finished printed page may be reproduced on any office copying machine.

The electronics allow the machine to produce copy at a rate of 180 lines/min, 5 lines/in (2/cm), with a 4.0″ (10.16-cm) print width on a 4.75″ (12.065-cm) roll of paper, and provides user software selection of 20, 40, or 80 columns. Data input is 7-bit ASCII, parallel input TTL levels, with strobe; acknowledge pulse indicates that data were received. Electrical requirements are 50/60 Hz, 115/230 Vac, 18 W for printing, and 12 W for standby.

Applications for the microprinter include production of hard copy from a CRT terminal, home/hobby computers, microcomputer development systems, diagnostic systems, demand message printing, and industrial instrumentation applications. It is also expected to be used as a punched card interpreter and unattended station logger. Initial deliveries of the $595 printer are planned for the last quarter of 1977.

Circle 172 on Inquiry Card

Complete Development Is Rapidly Obtained From µProcessor System

Omnibyte Corp, 900 Jorie Blvd, Oak Brook, IL 60521 has based the modular 6800 microprocessor development system on their bus-oriented system that includes both analog and digital I/O. With the development system, the operator can progress from source code entry, editing, and assembly through debugging and checkout of RAM resident object code. Other features include p/ROM programming capability and expansion allowing incorporation of various peripheral equipment such as tape readers, punches, and printers.

The system consists of a 16-slot card file; power supply; seven cards for program development—CPU, controller, ACIA, 8k RAM, 2k RAM/4k ROM, and p/ROM programmer; nine slots for user hardware interface; terminal; and dual-spindle floppy disc system. Software includes an FDOS II Executive, resident disc driver, editor, assembler, p/ROM programming routine, and Omnibug terminal monitor.



Components of Omnibyte microprocessor development system are power supply, 16-slot card file with seven program development cards, dual-spindle floppy disc system, p/ROM programming routine, and optional Texas Instruments model 743 terminal

Circle 173 on Inquiry Card

µComputer Development Equipment Is Offered On Rent/Lease Basis

Staffed with development hardware specialists and engineers, Microcomputer Rentals, 1562 Devonshire Ave, Westlake Village, CA 91361 specializes in the rental and leasing of microprocessor development hardware exclusively. Available hardware includes Pro-Log p/ROM programmers and system analyzers; Intel Intellec MDS and 8080, 4040, and 4004 development systems; and Motorola EXORcisers, as well as related support equipment for each.

Equipment is rented on a weekly or monthly basis; leases are available for a longer term. Also offered is a provision to purchase used equipment.

Circle 174 on Inquiry Card

Software Disassembler Enhancement Uses Little Memory Space

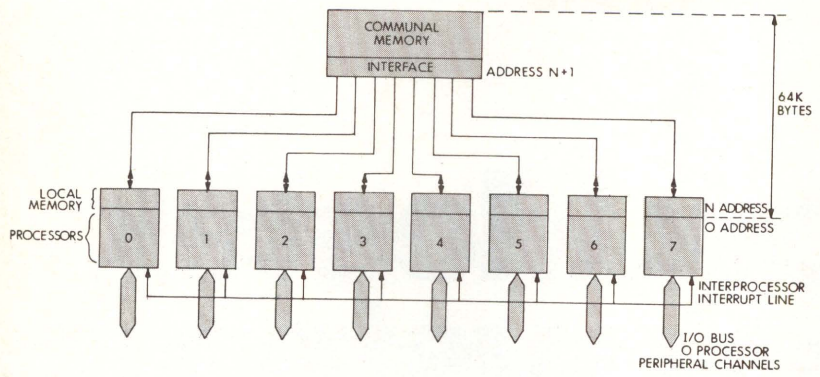
MIKADOS + D, announced by Inpro Micro Systems, PO Box 7776, Van Nuys, CA 91409, retains all features of the MiniInstant Keyboard Assembler, Debug, and Operating System (MIKADOS), while adding a complete disassembler to ease assembly, debugging, and modification of programs using a small amount of memory. It occupies only 3k bytes of memory, leaving 1k bytes for user programs and label table.

The assembler generates object code for 72 basic variable-length instructions with all addressing mode variations, enters user mnemonics into user program memory, and outputs formatted object code and address on the same line as user input. Relative addressing for branch instructions with symbolic labels are resolved and a label table is maintained. There are 18 useful directives online at all times, providing interactive capabilities which include disassembly of object code into source code with complete instruction mnemonics and absolute branch addresses.

Circle 175 on Inquiry Card

Up to Eight Separate µComputers Are Combined to Form Federal System

Offering solutions to problems normally allocated to large, real-time



Micral M System can be configured with up to eight microcomputers which operate with separate I/O buses, memories, and interrupt systems, as well as with shared memory

computers when in its maximum configuration, Micral M is a federation of independent microcomputers (up to eight), each of which possesses an I/O bus, memory, and interrupt system. Within its addressing field each microcomputer has its own memory (inaccessible to others) and the communal memory. Also, each microcomputer can interrupt any of the processors.

The system from Réalisation et Etudes Electroniques, Zone d'activités de Courtaboeuf, Avenue de Scandinavie, BP 73, 91403 Orsay, France features no memory conflict between the processors working in parallel on individual tasks. Tasks transmit arguments through the communal memory; sharing of communal programs executed in the communal memory is transparent. All units are nonspecialized for flexibility and safety.

From one to eight Micral S microcomputers can be used in the system containing 6k to 510k bytes of central memory distributed between local and communal memory depending on the number of processors. Included are 64 high priority interrupt levels and 512 lower levels, with rates of up to 64 channels of 1M bytes/s, and approximately 2.5M instructions executed/s. Entry addressing has 16,384 bits; output addressing has 6144 bits.

In its minimum configuration, the system fits applications requiring a number of single-processing micro or minicomputers. Configurations can be added onsite without affecting hardware or existing equipment.

Circle 176 on Inquiry Card

Microprocessor System Features Integrated Floppy Disc Memory

The S-100 bus Horizon™ computer includes a full speed (4-MHz) Z80 microprocessor, 16k bytes of memory, disc controller with Shugart minifloppy™ disc drives, 12-slot motherboard, and heavy duty power supply. Disc operating system and full extended BASIC are contained on diskette for power-on bootstrap startup. A serial I/O port is included for connection to any standard baud-rate terminal. Chassis has a brushed aluminum front panel, with either wood or blue painted metal cover.

North Star Computers, Inc, 2466 Fourth St, Berkeley, CA 94710 has announced its entry into the microcomputer mainframe market with this system. The processor board with the Z80 also has a USART for synchronous or asynchronous serial I/O communications (RS-232 or current loop), and vectored interrupts. The 16k RAM board contains bank switching capability allowing expansion beyond 64k bytes. The micro disc system includes the S-100 interface board with bootstrap P/ROM, a disc drive, cabling, connectors, documentation, and two diskettes. Up to three drives may be controlled; in most cases power can be taken from the computer power supply.

Hardware floating point board implements add, subtract, multiply, and divide on BCD-format floating point values with up to 14-digit precision. Power supply provides 12 A at 8 V and 6 A total at ±16 V.

Horizon-1 includes the 16k RAM board and micro disc system with one Shugart minifloppy disc drive front-mounted inside the enclosure. Horizon-2 is a dual-drive configuration. For nondisc applications or those that already have a minifloppy disc system, Horizon-0 offers the chassis, cover, power supply, processor board, and motherboard. Cabinet dimensions are 7 x 19 x 17" (17.78 x 48.26 x 43.18 cm).

Options include additional disc drives, hardware floating point arithmetic board, 24-line by 80-char upper/lower case video display controller (VDC) board, and 16k memory board with parity check. The VDC also displays 48 lines by 80 char and high resolution (480 by 250) graphics on a TV monitor. Other peripheral products can also be used with the computer.

Circle 177 on Inquiry Card

LSI-11 Serves As CPU for Ready-to-Use Computer

A complete computer that utilizes the DEC LSI-11 CPU and 56k bytes of RAM, the PRD11 from RAD, Inc, 5012 Herzel Pl, Beltsville, MD 20705 is packaged in a 23-lb (10.43-kg) suitcase configuration. The unit has provisions for multiple terminal interfaces, a mass memory interface, and a data acquisition subsystem. All system power supplies feature overload and short-circuit protection.

The computer is available with a Computer Operations portable Linc Tape mass memory that is compatible with DEC's RT11 operating system. Available software includes full macro assembler, FORTRAN IV, Multiuser BASIC, FOCAL, and APL.

Anticipated applications include educational uses in which the system supports up to four BASIC language users, and data acquisition uses in which up to 64 channels of analog information and 64 channels of digital input may be accommodated. Configuration flexibility is obtained with system options and peripheral choices.

Circle 178 on Inquiry Card

MK4098
MK4027 MK4116
MK4104

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MK 8003. Mostek Memory System's add-in memory card for the Data General Nova 3. This memory card provides up to 128K x 17 of storage on a single 15″ x 15″ printed circuit board, and uses Mostek's reliable 4116 16K RAM technology. The 8003 is completely compatible in both hardware and software with the Nova 3/4, 3/12, or 3/D. Smaller capacities are available.

MK 8000. The MK 8000, a 128K x 24 single-card system, uses Mostek's 16K dynamic RAMs for lower power and greater system reliability. The system is pin-compatible with industry standard core and semiconductor systems. Flexible operating modes (including page mode), low power (30 watts), high speed, and high density make the MK 8000 the industry's best value.

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For information on Mostek memory systems, contact your local sales representative or call Memory Systems Marketing at (214) 242-0444, ext. 554.

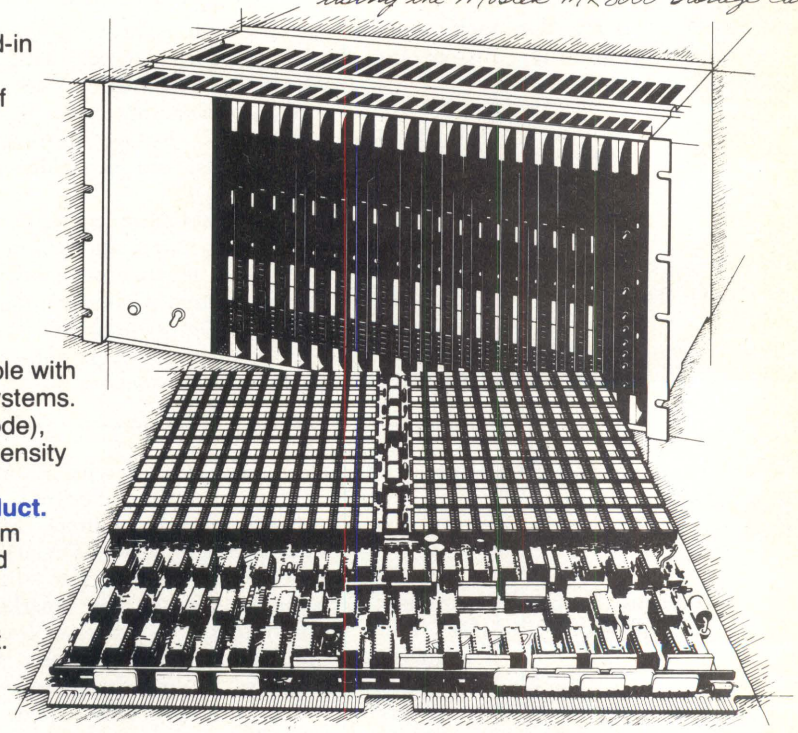
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High Speed Access: 250ns, Cycle: 450ns.

Low Power 25 Watts Typical

I/O (Separate or Muxed DATA/ADDRESS)

CIRCLE 68 ON INQUIRY CARD



Very little stands between your mini and the disk drives of your choice.

Just Telefile's little Matchmaker disk controller. With it, we can put your minicomputer together with *any* of the latest 3330-type disk drives: Ampex, Memorex, CalComp, Control Data, or Diablo. You'll have a system no one else can match.

Greater flexibility.

Special tailor-made, compatible interface modules make changing minicomputers a snap.

To change drives, simply switch circuit boards. Capacity can grow from 13.3 million to 1.2 *billion* bytes per system.

Interface software included.

Telefile even provides handlers that make the Matchmaker software transparent to the operating systems of most major minicomputers.

Unmatched features.

Telefile's Matchmaker controller brings to minicomputer users the latest large mainframe disk technology with such features as: *Search and read command* to help you with data base management. *Write protection* to the sector level. And *Advanced error recovery* techniques.

The Matchmaker even comes with a separate maintenance module for offline disk pack formatting and test exercising.

And Telefile stands behind the system not only with hardware and software, but with nationwide service support in major metropolitan areas.

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100 fact-filled pages on the universal Matchmaker concept including operation, functional specs, features, diagnostics, installation, and maintenance. Get it free by writing: Telefile Computer Products, Inc., 17131 Daimler St., Irvine, CA 92714. Or call toll-free (800) 854-3128. In Calif., (714) 557-6660.

Telefile

Enhancing computers is our business.

CIRCLE 69 ON INQUIRY CARD

32k-Byte RAM Is Expandable, Modular Board for Hobbyists

Compatible with the S-100 data bus and speed-compatible with Zilog Z80-based systems, the 32k-byte static memory board in modular form is designed primarily for microcomputer hobbyists, but is also applicable for small business uses. Requiring only a single 8 V with power usage of 3 A, the 32k-100 board has an access time of 250 ns. DMA compatibility allows access without going through the CPU on the microprocessor board.

The board is fully buffered on all address and data lines. Features include battery backup and a "bank select" provision permitting selection of blocks (or banks) of memory to be addressed.

Artec Electronics, Inc, 605 Old County Rd, San Carlos, CA 94070 is offering the basic board with all support circuits, power regulator, 8k bytes of memory, and assembly manual for $290. Additional 8k bytes of static RAM cost $255 each; a full 32k board sells for $1055.

Circle 179 on Inquiry Card

Nonvolatile Data Memory For Single-Board Computer Warns of Power Failure

A packaged solution to data memory volatility problems has been developed for the SBC 80 single-board computer family and System 80 OEM computers with a technique that also gives system central processors "early warning" of power failure so that critical data can be saved in standby memory. The SBC 094 4k-byte CMOS RAM and battery backup board, introduced by the OEM Computer Systems Group of Intel Corp's Microcomputer Div, 3065 Bowers Ave, Santa Clara, CA 95051, measures 12 x 6.75 x 0.6" (30.48 x 17.15 x 1.27 cm) including battery pack height.

Maximum cycle times are 730 ns for read and 800 ns for write. Supply voltage is 5 V ±5% with typical supply current of 0.8 mA and maximum current of 1.7 mA in active operation. This power input is also used by an onboard battery charger for the nickel-cadmium battery. Standby supply is 3.6 V with a capacity of 150 mAh. Overcharge and short-circuit protection are included.

Multiple processors can share the same CMOS memory through the company's Multibus™ bus structure. Up to 16 "masters," such as SBC 80/20 single-board computers, can use the board or it can be dedicated to a single master, such as the SBC 80/10. In addition to standby, the memory can be used for low power expansion of the main data memory on one or more SBC 80 computers.

Giving any SBC 80 CPU ample time to transfer critical data to the CMOS RAM is the memory's early warning technique and the standard SBC 635 power supply unit which generates an ac-low signal if line voltage drops (manufacturers can provide ac-low detection in their power supply design). The supply has enough capacitance to maintain dc supply levels within tolerance long enough for interrupt, data transfer, and shutdown operations to take place.

Upon detecting the signal, the memory generates the interrupt; 3.6 ms after it receives the ac-low signal it also generates a memory protect signal. This disables read/write access to protect the RAM's contents during shutdown.

When the 5-V supply fails, the onboard battery pack takes over with sufficient capacity to power the RAMs for at least 96 h. Automatic recharge of the battery occurs when system power is restored. The company's 5101 256 x 4 CMOS static RAMs, which require only nanoseconds of current on standby, are used on the board which is available for $795 in single quantities.

Circle 180 on Inquiry Card

Module Provides Powerful Interface Between PDC Family and Peripherals

A 24-bit I/O card designed to be bus and card size compatible with the National ISP family of cards and the company's PDC (Programmable Data Controller) family of microprocessor cards provides a powerful interface between the microprocessor and external devices. Developed by MilerTronics, Div of George Miler Inc, 303 Airport Rd, Greenville, SC 29607, the PDC-440 is capable of being user-modified to conform to any type interface desired.

Three 8-bit latched data output ports and three 8-bit data input ports provide capabilities for interfacing the system to up to three peripherals requiring 8-bit parallel data transfer. It may also be used as a parallel I/O port with up to 24 bits. If more than 24-bit parallel capability is required, additional modules can be added to the system. Address of each I/O module is selected by installing the appropriate set of jumpers.

Other features include asynchronous data transfer I/O handshake controls, interrupt controlled data transfer capability, programmable card address permitting multiple cards/system, and wirewrap section for user-supplied interfaces. Minimum power is obtained through extensive user of low power Schottky technology. A 72-pin edge connector plugs directly into the PDC backplane, and two 36-pin I/O connectors have user definable pinout on the opposite side of the card for interfacing to the system peripherals.

Data transfers can be handled totally under system software control or in an interrupt driven mode. Independent transmit and receive interrupt logic is provided.

Circle 181 on Inquiry Card

Moving Head Disc System for LSI-11 Increases Addressable Data Base

The Phoenix 145 moving head disc system which operates with the DEC RT-11 operating system enables users to address a greater data base than is otherwise available with floppy discs. With a 10M-byte capacity, the disc drive is expandable to 40M bytes.

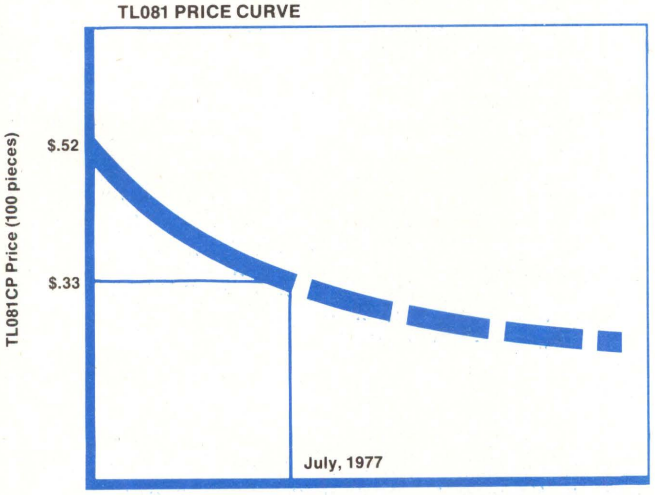
Complete system consists of a Phoenix C45L disc controller and power supply contained in a 5.25" (13.34-cm) chassis, an LSI-11 CPU, 28k bytes of semiconductor memory, power sequencing/terminator, and a DLV-11 serial interface enclosed in a 30" (76.2 cm) pedestal cabinet. Xylogic OEM Components Group, Inc, 42 Third Ave, Burlington, MA 01803 provides its own line printer controller and bootstrap loader for the system.

System can stand alone or accommodate other standard LSI-11 and 11/03 peripherals. OEMS and companies integrating small business systems or distributed processing networks can support up to 14 Q bus I/O devices, a line printer, and 28k-word LSI-11 processor in the 9-slot backplane.

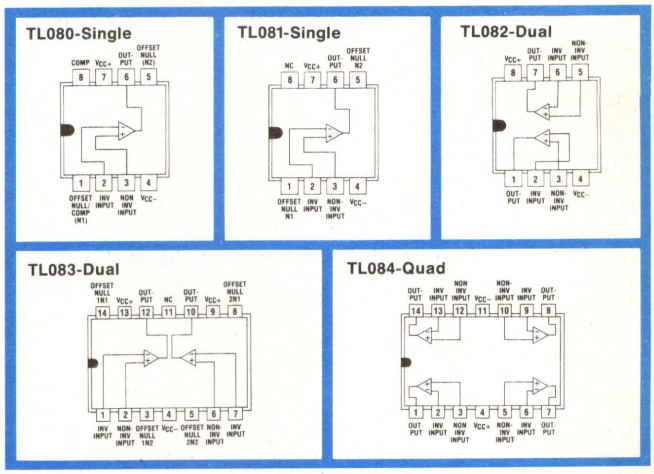
Circle 182 on Inquiry Card

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CIRCLE 70 ON INQUIRY CARD

Controller Interfaces IEEE 488 Devices to SBC 80 Computers

Operating as a controller for the IEEE Standard 488 interface (the GPIB for general-purpose interface bus and HPIB for Hewlett-Packard interface bus), the model ZT 80 self-contained intelligent controller matches the Intel SBC 80 computers electrically, physically, and logically, providing access to over 100 instruments and peripherals for the single-board computers. No detailed knowledge of the bus is required of the designer as the controller is programmed using a set of high level channel instructions and operates as a full parallel I/O processor to the SBC 80. Communication to the controller is accomplished via a 1k-byte shared memory area used to store channel programs and data buffers.

Using 4k bytes of onboard ROM and 1k bytes of RAM for buffering or general routines, the board from Zia Tech, 10762 La Roda Dr, Cupertino, CA 95014 also provides complete controller talker/listener capability. In operation, it multitasks sequences of high level commands placed in memory by an SBC 80 and performs all bus protocol required to communicate over the IEEE interface. Commands map into the 488 protocols, allowing the user to exercise the bus without manipulating each bit separately.

Currently available devices interfaced to the bus include printers, plotters, floppy discs, cartridge tape units, and a full range of electronic test equipment. The controller is priced at $950 in single-unit quantity.
Circle 183 on Inquiry Card

Conversion Program Eases Changeover from 8080 to Z80 Microprocessor

An 8080 to Z80 conversion program, announced by Microtec, PO Box 60337, Sunnyvale, CA 94088, converts standard Intel assembly language statements to equivalent Z80 statements, enabling users switching to the Z80 microprocessor to convert their programs at low cost and effort. All required mnemonics, reserved names, and syntax conversions are performed.

Features include detection and flagging of certain errors present in the 8080 input statements, control of field formatting in Z80 output statements, and output listing controls statements. The program, written in standard ANSI FORTRAN, runs on any computer regardless of word length.

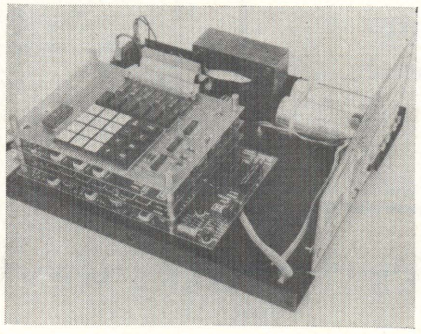
The program is priced at $300 when purchased separately; $50 when purchased with the company's Z80 cross-assembler. This includes source program on cards, magnetic or paper tape, and user's manual.
Circle 184 on Inquiry Card

Z80-Based Microcomputer System Features p/ROM Programmer

MIKE 8, a microcomputer system based on the Z80, has been added to the Modular Micro series of 5.5 x 7" (13.97 x 17.78 cm) microcomputer boards. Claimed by Martin Research, 3336 Commercial Ave, Northbrook, IL 60062 to be comparable with Intel's small development system, this system uses the Z80 extended instruction set which includes the 78 Intel 8080 opcodes, plus 80 others.

Model 882 comes with a 450-ns 4k RAM, a 1k monitor program in a p/ROM, CPU board, and "console board" which has a calculator-type keyboard and display of six LED digits. The monitor allows the user to enter and execute programs via the console; it also offers advanced debug features such as RAM test, single-stepping, and setting traps.

The system includes a p/ROM programmer for the user to permanently store programs in a blank 2708 1k x 8 p/ROM (which is included). An ultraviolet lamp is supplied for erasing p/ROMs.



The unit is mounted on a base with its own 5-V switching-regulated power supply. A "blackbox" enclosure allows the unit to be adapted to many industrial and hobby applications. The assembled system sells for $895.
Circle 185 on Inquiry Card

Second-Sourced COSMAC Circuits Are Available

A family of CMOS microprocessor components, second sources of the RCA CDP 1800 series, is being offered by Hughes Aircraft Co, MOS Products, 500 Superior Ave, Newport Beach, CA 92663, according to an agreement signed with RCA last year. First of the 8-bit LSI circuits, designed for numerous MPU applications, are the HCMP1802 CPU, HCMP1824 RAM, and HCMP1852 I/O port. The CPU provides system control, information handling, and computational operation; the RAM is organized as 32 registers of 8-bit words for use as temporary storage of data or instructions; and the I/O port acts as a buffer interface to adapt peripheral devices to the 1802 bus.

Other components in the 1800 family are scheduled for introduction over the next few months. Support software will also be made available for the various components.
Circle 186 on Inquiry Card

Card Extenders Aid Microcomputer System Design and Debugging

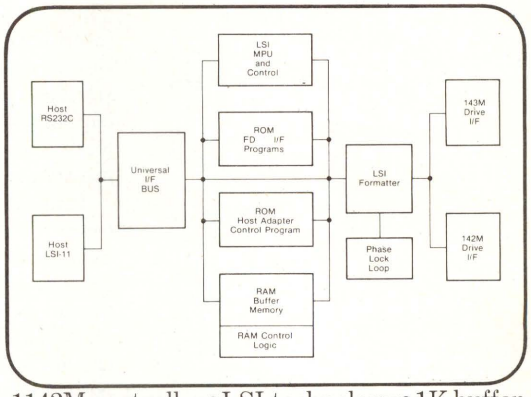
Model 3690-12, a 7.5 x 9.99" (19.05 x 25.37-cm) circuit card extender, is form- and plug-compatible with Altair 8800, Imsai 8080, and other similar microcomputer CPU, memory, and interface boards. Vector Electronic Co, Inc, 12460 Gladstone Ave, Sylmar, CA 91342 has introduced the device to facilitate out-of-chassis troubleshooting and hardware debugging.

Fully assembled units are fabricated of 0.0625" (0.159-cm) thick epoxy-glass composite material. The 2-oz (56.7-g) copper conductors are solder tinned while the card edge connectors are gold-flashed nickel plate for low contact resistance and reduced wear. Mating receptacle has 100 contacts (50/side) on 0.125" (0.3175-cm) centers. □
Circle 187 on Inquiry Card

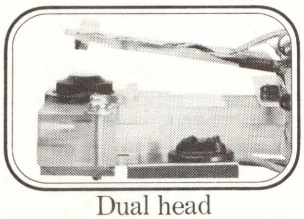
Meet the First Family in floppies.



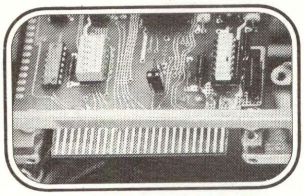
The roots of our floppy family



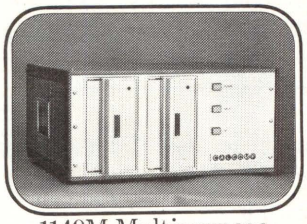
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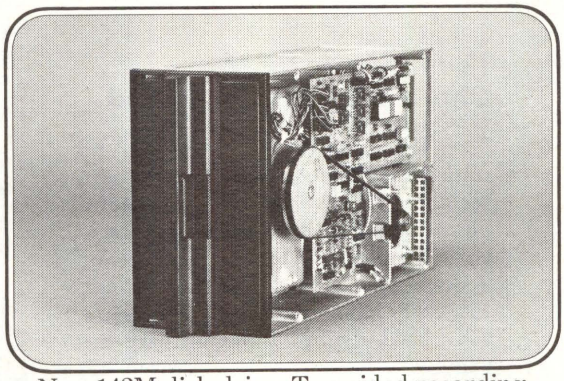
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AROUND THE IC LOOP

Display Drivers Provide Voltage Needed For Larger Vacuum Fluorescent Panels

To providing the voltage necessary to drive the large vacuum fluorescent panels now being used in POS terminals, DPMS, and automotive dashboard displays, Dionics, Inc, 65 Rushmore St, Westbury, NY 11590 has developed level-shifted vacuum fluorescent display drivers. For use as both digit and segment driver, 504/509/514 series devices are available in 4-, 6-, and 8-line versions.

Designed for interfacing with MOS or TTL inputs, the monolithic silicon dielectrically-isolated ICs have 50-V level shift capability and 50-V output capability. Each section of the device consists of a switched constant-current level shifter and a pnp-npn driver transistor pair. Provision for 50-V offers a high safety factor for the normal 35-V operation of the circuits. Output drivers exhibit a typical 1.5-V saturation at 10 mA of output current.

Prices at the 10,000-quantity level are quoted as $0.93, $1.10, and $1.22 for 4-, 6-, and 8-line versions, respectively. Delivery is from stock.

Circle 350 on Inquiry Card

Monolithic 8-Bit ADCs Operate at 400 ns

Two complete monolithic, 8-bit analog-to-digital converters capable of operating at conversion rates of 1 μs and 400 ns have been produced by TRW LSI Products, One Space Pk, Redondo Beach, CA 90278. Designated TDC-1002J and -1001J, the bipolar devices are 5-V, TTL-compatible.

Accurate within ±½ LSB, the highly linear devices can make complete A-D conversions at a 1M- or 2.5M-sample/s rate. They require a synchronizing clock signal, an accurate full scale reference voltage, and a compensating capacitor. Nine clock periods are required per conversion with a typical clock frequency of 22.5 MHz.

A status output indicates when the converter is available for the next conversion. All output bits are available one clock period after the status signal indicates "ready to convert." There are no missing codes. All digital interfaces are TTL-compatible, representing less than one-fifth of one standard TTL load on input. Fanout capability is two Schottky TTL output loads. 5- and −5-V power supplies are required.

Input full scale range is from 0 to −0.5 V. The 8-bit parallel output uses binary coding, with 0-V input giving a 0 output. A −0.5-V input produces a 255 output. An on-chip operational amplifier is used to buffer the full scale reference input. The "start convert" input is a D-type, positive edge-triggered range.

Prices are $75 each in 100 to 999 units for the 1 μs TDC-1002J; $175 each in 100 to 999 units for the 400 ns -1001J. Full military temperature range versions of these devices are planned for late this year.

Circle 351 on Inquiry Card

1k-Bit Static RAM Challenges Bipolar Speed

The 45-ns S4015-3, a 1024 x 1-bit static RAM, developed using V-MOS technology, provides competition for bipolar devices by offering MOS-compatible speed and price. By using V-MOS design, American Microsystems, Inc, 3800 Homestead Rd, Santa Clara, CA 95051 derives three primary advantages: high speed, increased LSI circuit density, and lower manufacturing cost.

Since device speed is critically affected by channel length, with short, wide channels having the edge, V-MOS has great speed potential. Channel length is simply the thickness of the p-layer, but channel width winds around the entire circumference of the V-groove, so that each transistor can transconduct several times more current per given unit of die surface area than a planar n-MOS transistor can. Cell size can be the same width as the connector lines to it, rather than larger, as in n-MOS.

Net result is a considerable increase in circuit density over both standard n-MOS and bipolar technologies. Analysis of the delays through the RAM indicate access time can be brought down to the 20 ns range, putting MOS technology ahead of second generation bipolar technologies.

A major point in the technology is that transistors are small enough to fit under the minimum size linewidth connectors formed. Transistors require no more room than is required to make connections to them. On a chip using the process, the smaller the lines, the smaller the transistors can be. Circuit density on such a chip exceeds that from any competing technology available or projected, primarily because of the additional vertical dimension.

Using V-MOS, for example, the upcoming 65,536-bit ROM on a 28,000 mil² chip is achievable. In addition, because the same basic cell design is used for ROM, p/ROM, and dynamic RAM, very high density ROMS, programmable ROMS, and RAMS are in design or prototype stages. Although the S4015-3, which will sell for $6.20 (in 100-up quantities), is the first part into production, others planned include a faster (30 ns) version of the 1k static RAM. Planned for fourth quarter 1977 production are the S4016 1k x 4 static RAM, S4017 4k x 1 static RAM, S6831-1 2k x 8 ROM, (available in popular 16k ROM pinouts), and the S4264 64k ROM (8k x 8).

Circle 352 on Inquiry Card

Monolithic V-F Converter Offers 12-Bit Linearity

Offering guaranteed 12-bit (±0.01%) linearity at 10 kHz and operation to 0.5 MHz, the VFC32, a monolithic voltage-to-frequency converter, is priced below similar converters that provide only 9-bit (±0.07%) linearity. Introduced by Burr-Brown Research Corp, International Airport Industrial Pk, PO Box 11400, Tucson, AZ 85734, the device can be used as either a V-F or F-V converter, and has a 6-decade dynamic range from 0.5 Hz to 0.5 MHz. Linearity at the top frequency is ±0.2% (8-bit), ±0.5% (10-bit), at 100 kHz.

The converter accepts voltage inputs of 0 to 10 or 0 to −10 V and current inputs up to 0.25 mA positive. Its open-collector output provides compatibility with DTL, TTL, and CMOS logic.

An external RC network sets up the full scale frequency, and one additional pull-up resistor and one-

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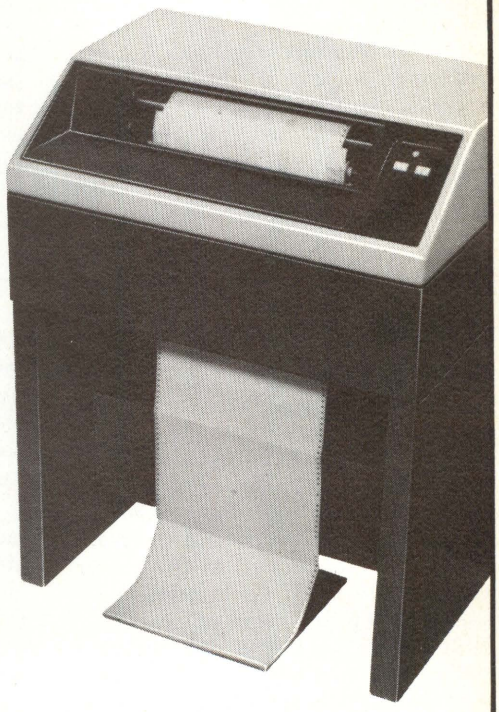
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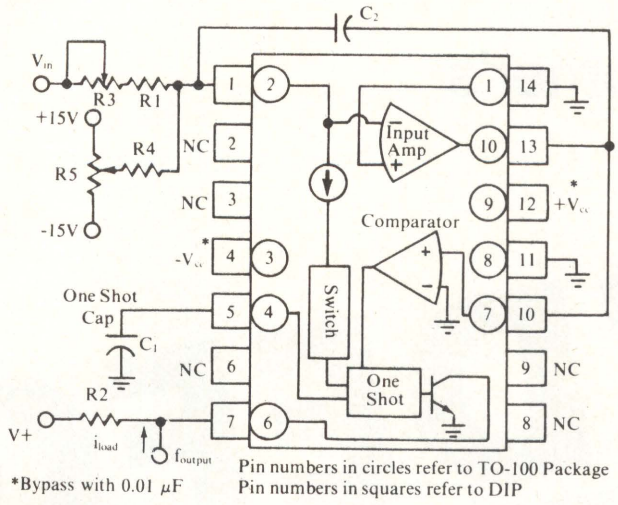
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CIRCLE 72 ON INQUIRY CARD



A V-F/F-V converter from Burr-Brown, VFC32 accepts either positive (connection shown) or negative input voltages, or an input current. Full scale frequency and input voltage are established by R1, C2, and C1 values

shot capacitor are required for operation. Tempco of the full scale accuracy is ±100 ppm/°C max; input offset voltage drift is ±2 ppm/°C.

A 14-pin epoxy DIP specified from 0 to 70°C (KP) and hermetically sealed TO-100 packages specified over the −25 to 85°C and −55 to 125°C ranges (BM and SM versions) are available. Prices in quantities of 100 to 249 are $6.10 (KP), $8 (BM), and $11.70 (SM).

Circle 353 on Inquiry Card

IC Decoder/Driver Simplifies 4-Digit LCD Interface

DF411, a 4-digit BCD-to-LCD decoder/driver IC, contains all circuitry needed to decode up to four digits of multiplexed BCD information and to create the ac signals required to drive four LCD display digits. Each device consists of a BCD to 7-segment ROM, four 7-bit latches, and on-board oscillator control logic; only one external component, an oscillator capacitor, is required for operation.

Output signals are 50% duty cycle square waves and contain no dc component to degrade display lifetimes. CMOS construction allows easy interface to systems using CMOS or open-collector TTL outputs.

The device reduces both system size and complexity. Driving a 4-digit display previously required four 16-pin packages and a 14-pin package; the DF411 reduces this to one 40-pin plastic DIP. Fewer interconnections mean increased reliability and better final assembly yields.

On-board control logic allows interfacing with systems which incorporate interdigit blanking. Four individual digit strobe input lines allow entering BCD data in any order desired by the user. Power consumption is 1.5 mW typical while driving a typical 4-digit 0.5" (1.27-cm) LCD. On-board latches allow instruments such as sampling (powered on for only a short time) DVMs to be built which can further extend battery life.

Pinout allows easy PC connection between driver and DIL as well as edge connecting types of LCDs. One example is the construction of a display board which is only slightly larger than a DIL display. This is done by placing the decoder/driver directly under the display. Input to the display board is accomplished via an 18-pin edge connector—an improvement over the 40-pin edge connectors needed in the past.

Available from Siliconix Inc, 2201 Laurelwood Rd, Santa Clara, CA 95054, in a 40-pin plastic DIP, the device is rated for operation over the 0 to 70°C range. Price is $6.49 in 100 to 999 quantity.

Circle 354 on Inquiry Card

MOS 4k Dynamic RAMs Win JAN Approval

Joint Army Navy (JAN) approval has been granted to MOS 4k dynamic RAM types TMS4050 and 4060. Qualification was granted by the Defense Electronics Supply Center authorization DESC-EQE-77-295 and is now listed in QPL 38510/28. These 4k RAMs, produced by Texas Instruments Inc, PO Box 1443, M/S 662, Houston, TX 77001, are the first LSI circuits to be qualified to JAN MIL-M-38510.

The ICs are described under MIL-M-38510/235 covering both 18- and 22-pin industry standard configurations in dual-in-line ceramic packages. They are guaranteed for operation from −55 to 85°C. Both the 4050 (18 pin) and 4060 (22 pin) are organized 4096 x 1 and feature simple non-multiplexed, fully decoded addressing utilizing a single clock to simplify system design. All inputs and outputs (except clock) are fully TTL-compatible, offering 200-mV minimum guaranteed dc noise immunity when interfacing with series 54, 54S, and 54LS TTL.

JAN versions of the TMS4050JR and 4060JR are designated JM 38510/23502BVC and JM 38510/23501BWC, respectively. Each is priced at $65.00 in 100-piece quantities. Availability is 16 weeks ARO.

Circle 355 on Inquiry Card

Digital Phase Lock Loop Achieved with Gate Array Technique

Successful design of a digital phase lock loop (DPLL) has been achieved using a digital IC technique, called universal gate array, at the Air Force Avionics Laboratory, Electronic Technology Div, Wright-Patterson AFB, OH 45433. Manufactured using LSI technology, the chip has the po-

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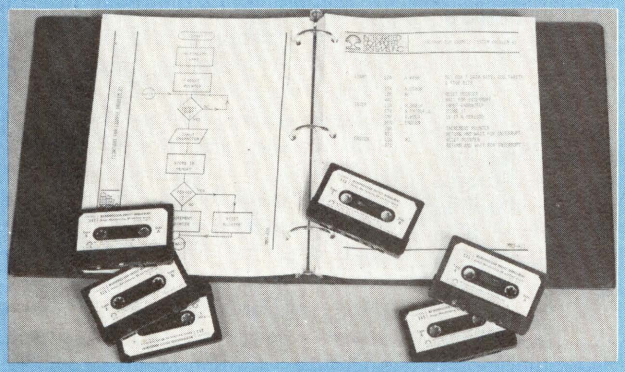
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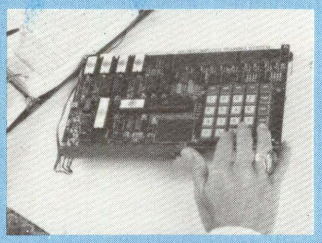
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SELF-STUDY MICROCOMPUTER SOFTWARE/HARDWARE TRAINING COURSE

COURSE 126

This new ICS Hands-On Training System is the first and only *SOFTWARE/HARDWARE* SELF-STUDY COURSE. The ICS Training System includes a fully-assembled 8080 microcomputer and built-in educational monitor program together with a coordinated 650-PAGE WORKBOOK/TEXT. The System is ready to use in your office or home (with its built-in keyboard/display, no expensive teletype or CRT terminal is required)! You will learn the details of both programming and interfacing by actually performing scores of exercises on your own microcomputer — at your own pace, in your office or at home.



The TRAINING COMPUTER includes: The 8080 microprocessor, .5K CMOS RAM, 1K PROM, three parallel I/O ports two serial ports, one DMA channel, and the on-board 8-digit display and 25-key keyboard.

The 650-PAGE WORKBOOK/TEXT includes 33 Hands-on exercises.

The ICS Monitor program is stored in the PROM memory and is specifically designed to be easy to use. It provides many unique functions essential to efficient learning. Furthermore, many monitor routines are available for use in your own programs, including display and keyboard I/O, timing, cassette interfaces, etc.

Using the ICS Training System, you will first learn each 8080 instruction through simple exercises which illustrate its effective use. These exercises, which also teach you basic programming, then progress to more and more advanced techniques. Other exercises specifically teach how to debug your programs quickly and effectively. Furthermore, throughout the course, hardware interface design and implementation projects are coordinated with programming problems. (For example, as your first project you will build a simple interface to an audio-cassette recorder.) Thus, you will learn both hardware and software design techniques and how to make HW/SW tradeoffs by actual hands-on experience.

KEY TOPICS COVERED IN COURSE:

• Introduction to the training system • Hardware fundamentals • Software fundamentals • The 8080 instructions — one by one • Using the keyboard/display to load and check programs • I/O programming — parallel/serial • Using a programmable I/O device • Interrupt handling (vectored/priority) • Organizing data in program (PROM) and data (RAM) memory • Subroutine structures • Real-time program design • Interfacing to a TTY, audio cassette, CRT • Advanced math routines (trig, logs, floating point, etc.) • Advanced I/O — block data and DMA use • Annotated work sheets for designing and implementing your own application

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CIRCLE 73 ON INQUIRY CARD

tential for being made inexpensively —to sell for about $3 to $4 as a standard catalog item—and performing many different functions in military and commercial applications.

According to Gary Gaugler, credited with designing the circuit, the universal gate array technique was chosen because it permits chips to be manufactured more inexpensively than a full custom approach. In using the technique, starting point is a universal or standard chip with many components. These parts, however, are not connected to one another or to anything else on the chip. What function is performed is determined by how the designer connects them.

A major advantage of the DPLL over analog phase lock loops is its adaptiveness. The chip can change frequency and/or bandwidth instantly. Among the functions the device is capable of are frequency tracking, bit timing, and data recovery in navigation equipment; and synchro/resolver-to-digital conversion in aircraft flight controls. Commercially, the device may find application as a replacement for demodulation and control circuit in mechanical disc drives in digital computers, for setting the automatic speed control on a car, or for use in commercial aviation.

Digital Monochip Eases Design of Custom ICs

A 138 x 138-mil chip designed to be converted into a custom LSI circuit with minimum engineering effort, the digital Monochip contains the equivalent of 262 gates and the potential for replacing 10 to 20 MSI packages. Developed by Interdesign, Inc, 1255 Reamwood Ave, Sunnyvale, CA 94086 in collaboration with Fairchild Semiconductor, the chip's unusual layout was achieved by concentrating on the basic cell. Rethinking its configuration permits the cell to be connected to perform any logic function.

With this cell as a building block, logic functions can be pieced together with simple geometric patterns. The process involves no design; if a flip-flop is needed, a transparency of that function is overlaid on the basic chip pattern, and the various function blocks are interconnected with pencil.

The chip uses an n-channel, silicon gate, isoplanar process. This process was chosen because it is more efficient than IIL. In addition, it permits cells to be connected into NAND or NOR logic, and provides levels that are directly TTL- and CMOS-compatible.

Tooling charge for the Monochip is a constant $2800; first 50 prototypes require four weeks. Other chips, having up to 1000 gates, are planned in the series.

Circle 356 on Inquiry Card

1k Static RAMs Surpass Speed-Power Performance Of Bipolar Devices

Surpassing the bipolar RAMs which they replace in speed-power performance, the 2115A/2125A and 2115AL/2125AL 1024-bit static MOS RAMs match the 45-ns speed while consuming 20 to 50% less power. The fully static devices, with equal access and cycle times, can directly replace the bipolar devices.

Pin-compatible and functionally interchangeable with bipolar devices, the RAMs from Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051 have standard 16-pin configuration and operate on a single 5 V supply at TTL levels. The 2115A has an uncommitted collector output and the 2125A a 3-state output. The 2115A features an output sink current of 16 mA, providing the full TTL fanout of 10 TTL loads. Fully dc stable (static) decoding and storage arrays on the chips eliminate the need for clock, strobe, or refresh operations, and allow system cycle times to equal access times.

Specifications guarantee that the basic series will match the 45-ns access time of the 93415/93425. This guarantee applies over the 0 to 75°C temperature range with the standard TTL supply tolerance of 5 V ±5%. Maximum supply currents are guaranteed at 125 mA for A versions and 75 mA for AL devices. Prices (100 quantities) are $7.40 each for low power versions, $6.90 for standard devices.

Circle 357 on Inquiry Card

Converter Measures True rms Value of Signals

AD536 directly computes the true rms value of any complex input waveform containing ac and dc components. Introduced by Analog Devices, Inc, PO Box 280, Rt 1 Industrial Pk, Norwood, MA 02062, the monolithic device enables designers to add rms options to measuring instruments at low cost. Wide bandwidth extends measurement capability to 100 kHz with 1% error for signals above 100 mV.

Enabling true rms value of complex wideband ac signals to be measured with total error down to 0.2% of reading; the companion AD536J features maximum error of ±5 mV ±0.5% of reading. These accuracies can be improved by a factor of two with external trimmers.

A single external capacitor is needed to set the low corner frequency and determine the low frequency accuracy and ripple level, as well as response speed and settling time. Use of a 2-capacitor scheme can improve settling times tenfold for the same ripple level.

Packaged in hermetically sealed, 14-lead ceramic DIPs, and specified for operation from 0 to 70°C, the units operate from either dual or single power supply, with total supply levels from 5 to 36 V. Quiescent supply current is 1 mA. An auxiliary dB output can be set to 0 dB to correspond to any input level from 0.1 to 2 V rms, with a useful dynamic range of 60 dB.

In 100 quantities, the AD536J is priced at $9.95; the AD536K sells for $18.50.

Circle 358 on Inquiry Card

Internal Input Register Eases DAC Interfacing

DAC-HK series 12-bit hybrid D-A converters incorporate a level-controlled input storage register to ease interfacing with a computer's data bus. A load input terminal digitally controls the state of the DAC, having it either store or transfer the input data. Three versions provide binary, BCD, and 2's complement coding. Pin-programmable output voltage ranges include 0 to 2.5, 0 to 5, and 0 to 10, ±2.5, ±5, and ±10 V.

Designed by Datel Systems, Inc, 1020 Turnpike St, Canton, MA 02021, the device incorporates a precision zener reference circuit, reference control circuit, three quad current switches, fast output amplifier, and input register. Quad current switches, combined with a low tempco nichrome thin-film resistor network, which is laser trimmed for optimum linearity, result in excellent tracking characteristics. Resultant 2-ppm/°C differential linearity tempco provides guaranteed monotonicity over the operating temperature range.

Converters have an output settling time of 3 μs to ½ LSB for a 10-V

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With the 9830A/B, the EM-30 provides 2,048 more bytes of memory, is priced right, and is fully warranted for a year.

FAST BASIC ROMS

Infotek's FAST BASIC ROMS add to the machine instruction set where HP left off. These ROMS provide spectacular increases in the work throughput of your 9830A/B. For example, you can process arrays at speeds of 40,000 words per second, attain an I/O capability of 10,000 bytes per second, greatly increase the power of a 9880A/B disk system, and print from a buffer while computing.

By providing 46 additional functions, statements, and commands, the FAST BASIC ROMS give your 9830A/B the most powerful BASIC language repertoir short of $200,000 systems.

If you need FAST BASIC but don't have enough unused ROM slots, don't give up! You can install our FAST BASIC ROMS without losing any present capability. **Contact us, we'll show you!**

*A Product of Hewlett-Packard Company



HP 9830A/B with the Infotek FD-30 Mass Memory

Floppy Disk Memory System

The FD-30A provides 305K bytes of on-line data that can be searched 50 times faster than your present cassette system. Data throughput is actually four times faster than the 9880A/B Mass Memory. Best of all, no software modifications are required since the FD-30A obeys all cassette syntax.

The FD-30A is the optimum magnetic memory for the 9830A/B. It has the right capacity, speed, and price.

Prices that you'll appreciate

EM-30 Memory, 16K Words $4,600	
Less trade-in of HP 8K Words 1,100	net $3,500
FAST BASIC I ROM	675
FAST BASIC II ROM	525
FAST BASIC I & II as a set	1,050
FAST BASIC III ROM	525
FD-30A Mass Memory	3,895
FD-30S Slave Drive	1,780
FD-30D Dual Drive System	4,900
RS-30 High Speed RS 232C Interface	750
TC-30 Real Time Clock	825
LP-30 Heavy Duty Line Printer	6,850
CP-30 Character Printer	3,400
PS-30 Paper Tape Punch/Reader	3,850
BP-30 Interrupt Service Printer I/O	525
FI-30 10K Byte/Sec TTL I/O	395

All Prices Are U.S. Domestic

NEW! The FD-30S low cost Slave Drive for the FD-30A. Multiple slaves can be used with a single FD-30A so you can increase on-line capacity in blocks of 305K bytes. Also, the FD-30S provides one minute disk duplication under program control or stand-alone.

NEW! BP-30 automatic buffered printing. Your '30 will **continue program execution** while driving a printer as a background task under interrupt control.

Save $2,100

In our Word Processing Package you get the EM-30, FD-30A, FAST BASIC I and III ROMS, and the CP-30, including software, for a special package price of $10,850.

Other 9830A/B Accessory Equipment

RS-30 High Speed RS 232C Interface. Provides seven crystal controlled Baud rates from 150 to 9600/sec.

TC-30 Real Time Clock. Provides time in 10-millisecond increments, is set or read via the OUTPUT and ENTER statements.

LP-30 Heavy Duty Line Printer. A 200 line-per-minute, 132-column printer (128 character set is standard). Comparable in every way to the 9881A, except the LP-30 is lower in price.

CP-30 Correspondence-Quality Character Printer. Provides 14 easily changeable fonts including scientific symbols, UK, German, Scandia, and Cyrillic. Prints and plots at 45 cps.

Contact us direct or through our representatives. Infotek products are sold and serviced through 33 offices in the U.S. and 11 in other countries.

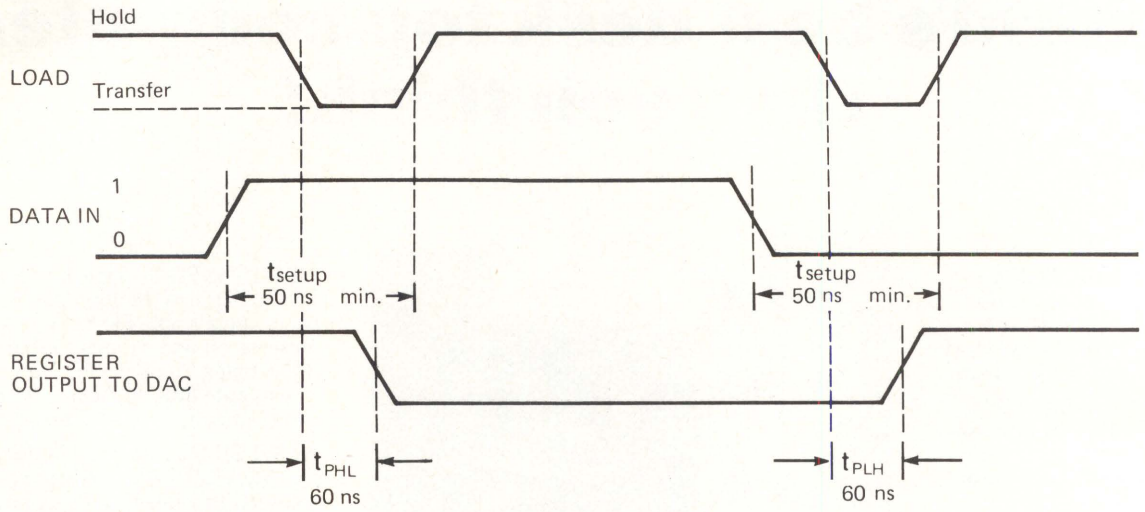
Let us show you how to make your '30 the best desk top computer in the world.

Infotek Systems

1400 N. BAXTER STREET • ANAHEIM, CALIF. 92806
(714) 956-9300 • TWX 910-591-2711

U.S. and Worldwide Distributor Inquiries Are Invited.

CIRCLE 74 ON INQUIRY CARD



Datel's HK series hybrid DAC contains a 12-bit input storage register as an interfacing aid. Load input terminal digitally controls state of the DAC, having it store or transfer input data

change. Linearity and differential nonlinearity errors are ±½LSB maximum. Gain temperature coefficient is 20 ppm/°C maximum. Power requirement is 15 V at 15 mA, −15 V at 30 mA, and 5 V at 45 mA; total consumption is 900 mW.

Prices for binary and offset binary coded devices in the 0 to 70°C temperature range are $99 in glass case, $109 in metal. Metal packaged devices in the −25 to 85°C temp range sell for $149; in the −55 to 125°C range, they are priced at $179.

Circle 359 on Inquiry Card

V-F-V Converter Operates from 0 to 1 MHz

A monolithic voltage-to-frequency converter, the A-8404 operates from a single 5- to 18-V power supply. In addition to linear conversion of 0- to 10-V analog signals into a proportional 1-MHz digital pulse train, the device can perform frequency-to-voltage conversion.

Requiring only six external passive components for interface, the unit can accomplish transfer functions over the full range with the equivalent of 8-bit accuracy by tailoring three of the external components. Linearity is ±0.4% max, gain tempco is typically ±200 ppm/°C, and output drive (V-F mode) is 20 mA at 1-V saturation.

Packaged in a 14-pin ceramic DIP, the unit provides DTL/TTL- and CMOS-compatible output. Devices are available from Intech/Function Modules Inc, 282 Brokaw Rd, Santa Clara, CA 95050 at a unit price of $12.

Circle 360 on Inquiry Card

4k Dynamic RAMs Offer 250-, 200-, or 150-ns Access

MCM4027, a 4096-bit dynamic RAM, is organized 4096 x 1 and fabricated using n-channel silicon gate technology to optimize speed, power, and density tradeoffs. Motorola Semiconductor Products Inc, 3501 Ed Bluestein Blvd, Austin, TX 78721 has tailored the device to provide 250-, 200-, or 150-ns access time.

Multiplexing row and column address inputs necessitates only six address lines and permits the device to be packaged in a standard 16-pin DIP. Complete address decoding is done on-chip with address latches incorporated.

All inputs are TTL-compatible and output is 3-state TTL-compatible. One-transistor cell design and dynamic storage techniques are incorporated; each of 64 row addresses requires a refresh cycle every 2 ms.

Circuitry of the device is largely dynamic so power is not drawn during the whole time the address strobe is active, making dynamic power a function of the operating frequency rather than the active duty cycle. Power dissipation is typically 470 mW active and 27 mW standby.

Pricing for 100-up quantities in hermetic package is $8.10, $8.50, and $10 for 250-, 200-, and 150-ns access times, respectively. In plastic, they sell for $6.60, $6.90, and $8.20.

Circle 361 on Inquiry Card

Data Acquisition System Multiplexes 16 Channels

A CMOS-compatible data acquisition system with 3-state logic on parallel output lines for CPU bus interface, the ZMP-2000 multiplexes 16-channels of real-time data from prime sensors and converts it to digital form. To provide total self-contained operation, Zeltex, Inc, 940 Detroit Ave, Concord, CA 94518, built sample and hold amplifier, 16-channels of FET multiplexer switches, 12-bit ADC, and all timing and control logic into the module.

Housed in a 3.0 x 4.6 x 0.375" (7.6 x 11.7 x 0.953 cm) shielded metal case with 72-pin connector, the unit operates over the 0 to 70°C temperature range with guaranteed monotonicity. A-D conversion time is 20 μs max, adjustable to throughput rates up to 33,000 channels/s. Differential linearity is $<\pm 1$ LSB with no missing codes.

Circle 362 on Inquiry Card

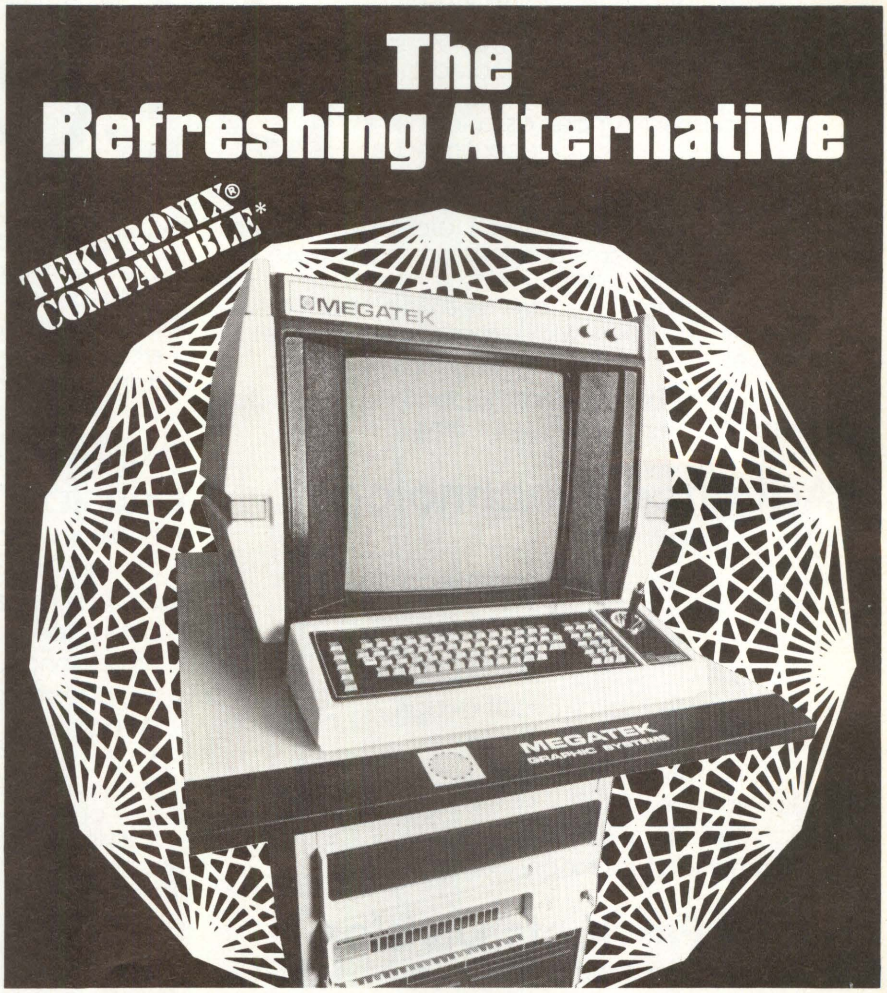
Line Drivers/Receivers Meet EIA Specs

Quad line drivers and receivers introduced by Advanced Micro Devices Inc, 901 Thompson Pl, Sunnyvale, CA 94086 are designed for driving long lines at rates of better than 10M baud. For use over commercial and military operating ranges, the circuits are packed in 16-pin molded and ceramic hermetic DIL and flat packages.

Am26LS31 is a quad differential line driver meeting all requirements of EIA RS-422 and Federal Standard 1020 for transmission of digital data over balanced lines. Low power Schottky technology provides typical skew of 2 ns between outputs at a propagation delay of 12 ns. A single 5-V supply is required and the 3-state output configuration ensures that devices do not load the line if the power supply drops to zero. The device is capable of driving a 50-Ω terminated transmission line.

A quad line receiver that meets both EIA RS-422 (differential) and RS-423 (single-ended) specifications as well as Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission, Am26LS32 has input sensitivity of ± 200 mV over an input voltage range of ± 7 V. Am26LS33 is a similar receiver intended for application in high noise environments such as aircraft bus systems. It features input sensitivity of ± 50 mV over a ± 15-V common-mode range. Both receivers feature a fail-safe I/O relationship. Outputs remain high when inputs are open. Three-state drive with complementary output-enables is provided for direct interface with a data bus. Prices start at $2 for the molded package in 100-unit lots. All three devices will also be manufactured by National Semiconductor under a second source agreement. □

Circle 363 on Inquiry Card



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Local Intelligence • Full Refresh • Zoom, Rotate, Translate • Sharp, Bright Vectors • Powerful Minicomputer • FORTRAN Software • Data Tablet or Joystick • Low Cost

Our Systems are Powerful, Intelligent, and Good Looking... the features YOU look for in a graphics terminal, system or interface. Coupled with MEGATEK Quality and Value, the picture is perfectly clear—MEGATEK is The Refreshing Alternative.

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Telephone: (022) 32.97.20
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CIRCLE 75 ON INQUIRY CARD

Engineers

Technological Leadership for 3 Decades!

Ampex, headquartered on the San Francisco Peninsula, is the company that "invented" the magnetic recording industry.

The technology pioneered by Ampex over three decades has affected many aspects of our modern lifestyles, and has established Ampex as a leader in magnetic recording. Our continued effort in developing new technology has always been the key to our leadership. Right now our Advanced Technology, Data Products and Audio-Video Systems Divisions are embarking on several new programs. To insure the success of these programs we are seeking innovative graduate engineers with experience in the fields listed below.

Opportunities like this don't happen very often. But they're happening at Ampex now.

Advanced Technology Division

- electron beam and optical recording
- magnetic recording
- tape or film handling
- servos
- high-bit rate digital circuit design
- optics
- signal analysis
- pattern recognition
- high frequency circuit
- communications theory

Data Products Division

- circuit/systems design of very high-bit rate systems
- disk read/write systems and equalizing systems for tape recorders
- codes for magnetic recording
- precision servo systems for both linear positioners and rotating systems
- mechanical design of high precision systems in disk recorders and in longitudinal, helical and transverse scan tape recorders

Audio-Video Systems Division

- analog videotape signal systems
- digital video signal processing
- servo systems
- videotape editing
- professional audio recorders
- head technology
- TV cameras

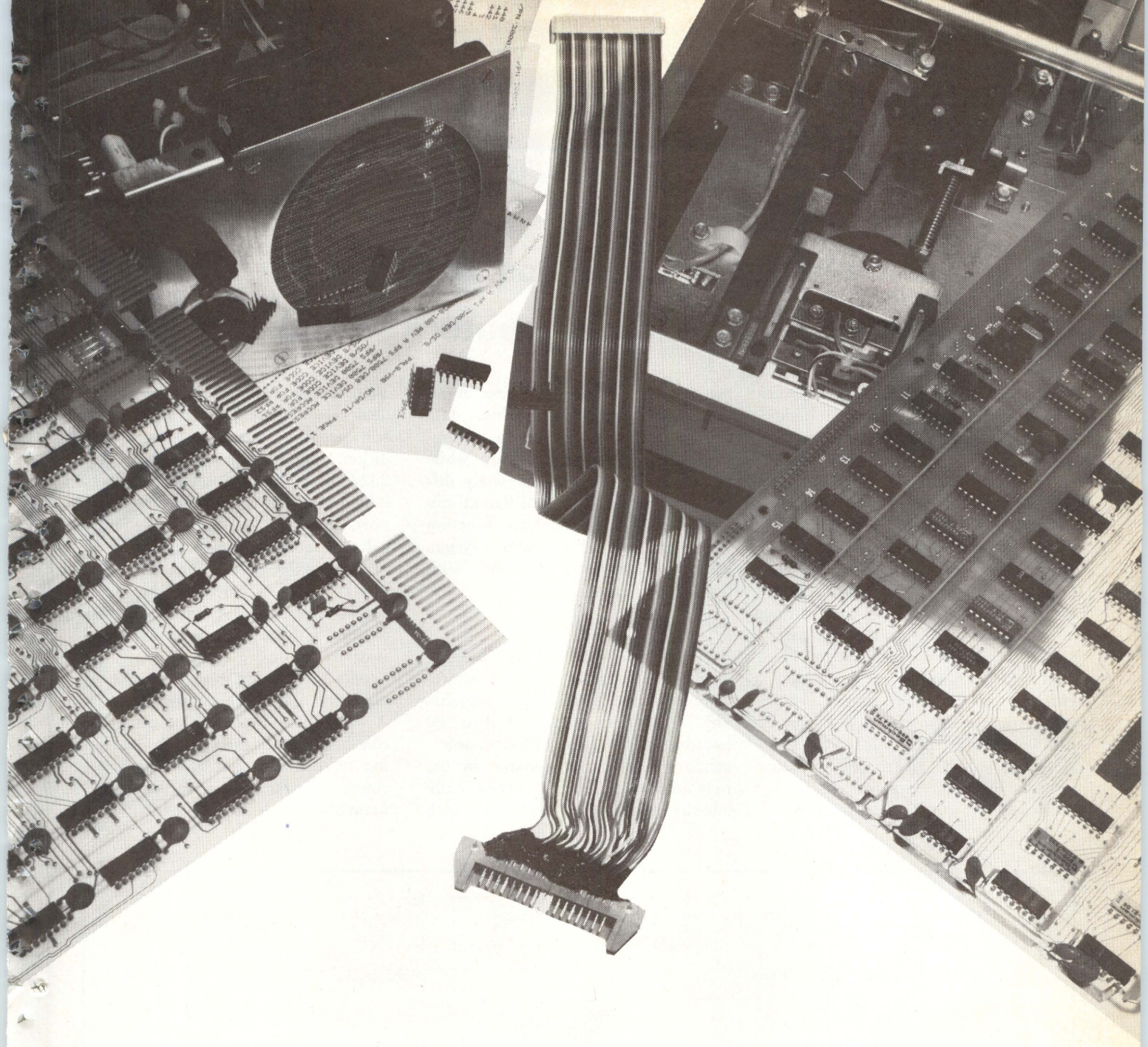
If you think you have something valuable to offer in any of these or closely related areas, and if you would like to join some of America's most talented engineers, please send your resume or a letter outlining your qualifications to: Ampex Corporation, ATTN: Corporate Staffing Manager, Building 2, 2655 Bay Road, Redwood City, CA 94063. Or you can send us this coupon and we'll get back to you. We are an equal opportunity employer m/f.

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AMPEX

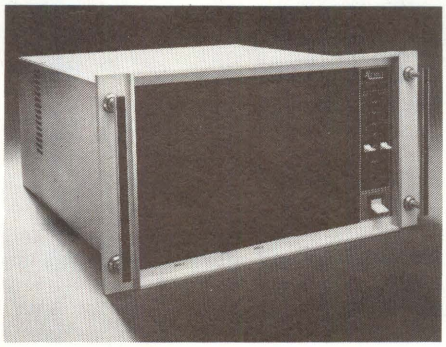


DON'T GO TO PIECES. GO TO REMEX.

A cost/effective OEM flexible disk system can't be pieced together — hardware from one source, firmware from another, software from a third. Getting optimum performance at a low unit price requires design control to eliminate redundancy and volume production to reduce cost.

That's why Remex offers the RFS7500 Flexible Disk System — a complete system designed and built by Remex — including one to four Remex drives, a microprocessor based controller/formatter, software and interfaces for most major minicomputers plus power supply, cable and rack mountable chassis. The RFS7500:

☐ expands data capacity through implementation of IBM3740 format or a user selectable 1, 2, 4, 8, 16, 26 or 32 sector format. ☐ saves computer time by data block transfer of from one to 65K 2-byte words on a single command from the host. ☐ reduces core memory requirements due to automatic track and sector search and auto-initializing without software. ☐ simplifies operation and system integration by 8-command structure. ☐ saves space by housing interface card in the system chassis in some configurations. ☐ speeds access through 6 ms track to track speed plus unit select.



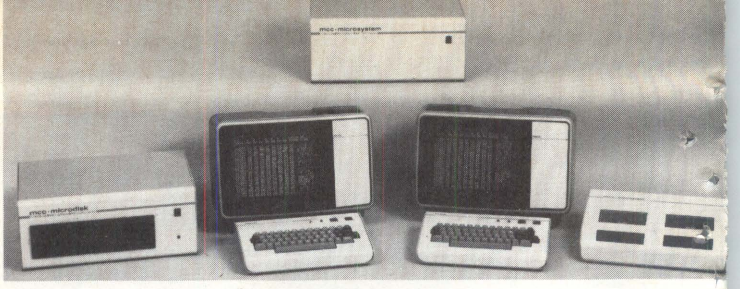
Ex-Cell-O Corporation

REMEX DIVISION

CIRCLE 76 ON INQUIRY CARD

The Remex RFS7500 is a better system at lower cost than the OEM can build himself or buy from a minicomputer manufacturer or second level supplier. Don't go to pieces, go to Remex, 1733 E. Alton St., P.O. Box C19533, Irvine, CA 92713 (714) 557-6860.

PRODUCT FEATURE



Dual System Develops Software for Two Independent Microcomputers At Same Time

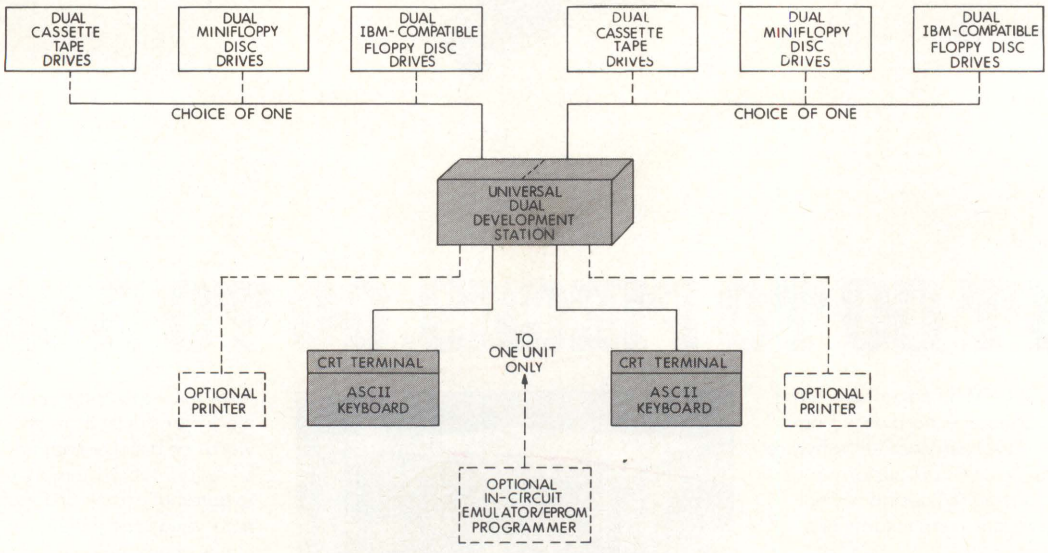
Two programmers now can develop microcomputer software simultaneously with the same unit—even for different types of microprocessors. The Universal Dual Microcomputer Development System offered by Microkit Inc combines two individually operating Microsystem development stations into one package. One programmer can work on 8080, 6800, or Z80 software while a second works on software for the same or another of the three processors. Price of the dual system, however, is three-quarters that of two single systems.

The dual system can also be used in a teaching environment where two students can be instructed on the same or different microprocessors simultaneously. Again, in manufacturing testing, industrial process monitoring and control, and business data processing, one side can be configured to a dedicated function while the other performs a completely different function with a different microprocessor. One side can function with one type of operating system while the other side functions with the same or another.

System Components

Basically, each side of the development system is a complete microcomputer: 8-bit central processing unit (CPU) made up of two PC boards; 8k bytes of random-access memory (RAM), expandable in 8k-byte increments to 32k bytes; cathode-ray tube (CRT) terminal with ASCII keyboard; dual mass storage devices and related operating system; software; and documentation. In addition, each includes dual EIA RS-232-C serial ports, real-time clock, 8-bit parallel TTL input/output (I/O) port, memory write-protect under software control, bootstrap loader in programmable read-only memory (P/ROM), vectored interrupt, and 1M-byte/s direct memory access (DMA) capability. Line printers can be added if desired.

CPU boards are based on one of the three applicable microprocessors. A switch to another microprocessor can be accomplished just by changing PC boards. Conversion packages consist of CPU boards, software, and manuals.



Dual Microsystem development system. Each half of dual station interfaces separately to CRT terminal and one dual mass storage drive; other unit interfaces to another CRT terminal and another drive—not necessarily of same type as used with first unit. One unit operates with 8080, 6800, or Z80 microprocessor while other unit operates independently with any one of the three microprocessors. Optional emulator/EPROM programmer can function with only one of two units at any given time

Each unit of the dual configuration contains five I/O channels: CRT interface, keyboard with miniconsole interface, dual tape interface, dual EIA RS-232-C interface, and 8-bit parallel I/O board. All I/O devices have maskable interrupts. The individual system bus is universal, with no card slots assigned to a particular peripheral device, controller, or CPU.

Program development is facilitated on each subsystem by the operating system software and assembler for the particular microprocessor. A unique characteristic is that commands for all operating system software except the assembler language statements are identical, regardless of which assembler is implemented. Thus, a programmer versed in 8080, 6800, or Z80 assembler language need learn the operating system commands only once to develop programs in any of the three languages.

Four operating system choices are available for each subsystem: cassette tape—including debugger/monitor, editor, assembler, and copy utility modules; Quickrun™—which has debugger/monitor, editor, and assembler co-resident in memory; and Microdisk™ small floppy and IBM-compatible standard-size floppy discs —both with disc monitor, debugger, editor, assembler, and disc utility modules. Extended BASIC is also available for the cassette tape or floppy disc systems.

The dual tape operating system (TOS) enables the operator to create a program file to contain the assembly language statements comprising the software being developed and to edit and debug the software until a working program is created. Thereafter, with the addition of an optional in-circuit emulator (Microemulator™), the program can be tested and debugged with the prototype hardware it will ultimately execute. This device is the only exception to the dual unit capability. It can be used with only one unit or the other at any one time. Dedicated software enables emulator mode, single-step and trace execution, hardware breakpoints, and 2708/2704 EPROM programming.

Editor software contains commands to insert source code; to position to a particular line of code; to insert, delete, and change lines of code amid existing lines; and to perform utility functions such as load and rewrite. Monitor/debugger software offers similar capabilities for object code. It can position to a block of code and commence execution; it can display a segment of code or patch new object code amid existing code. Moreover, it sets breakpoints, allows the user to single-step through a program, and provides a 20-step trace (saves the CPU register's state for 20 steps prior to breakpoint).

Quickrun requires 32k of RAM in place of the standard 8k supplied. It is memory-resident—which reduces program development time—and provides enough work space to contain a 1000-statement source program and a 4k object work area. In addition, it can write-protect any 1k-byte block of memory specified by the programmer.

The floppy disc operating systems provide development functions identical to those of the TOS. Both result in increased program efficiency because of the increase in speed, while the standard floppy system offers larger mass storage. (Average track-to-track access times and storage capacities of the minifloppy and standard floppy, respectively, are 260 ms and 160k bytes and 400 ms and 500k bytes.)

Still another option is a "Barebones" microcontroller made up of CPU, power supplies, p/ROM-ROM, and universal prototype board for customized I/O. Additional hardware and software can be chosen by the user for specific requirements.

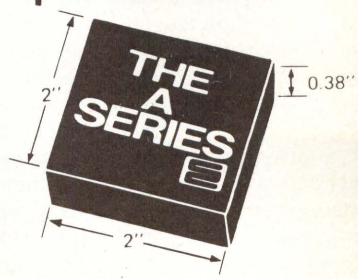
Price and Delivery

A basic configuration Universal Dual Microcomputer Development System, Microsystem/10/10 Mod 8080, consisting of two complete 8080 cassette tape-based 8k systems is priced at $5850. (Two separate systems would have cost $7700, or about one-fourth more.) 6800 and Z80 conversion packages are $950 each. An in-circuit Microemulator/EPROM programmer can be added for $1250 and an optional printer costs $2300. Alternate mass storage devices and operating systems are additional cost items. Quantity purchases of 100 systems receive a 35% discount. Delivery is 30 days ARO. Microkit Inc, 11205 S LaCienega Blvd, Los Angeles, CA 90045. Tel: (213) 641-7700.

For additional information circle 199 on inquiry card.

THE LOW PRICED DC/DC CONVERTERS. . .

that out-perform the higher priced brands



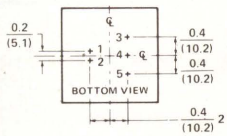
ONE LOW PRICE: $40.50 (1-249)

THE I/O RATINGS YOU NEED . . .

Input Voltage Vdc	Output Vdc @ mA	Model No.
5	±12V@±150mA	A5-12D150
12		A12-12D150
5	±15V@±150mA	A5-15D150
12		A12-15D150

QUALITY PERFORMANCE. . .
Regulation: 0.1% Line/Load
Efficiency: to 55%
I/O Isolation: 300Vdc Min.
MTBF: >100,000 Hrs.
Input . . .
Reflected Ripple: 1% Vin
Range: ±5%
Output . . .
Ripple & Noise: 20mV (typ)
Short Ckt. Protection: Yes

HERE'S THE PINOUT . . .



Pin 1 +Vdc in
2 -Vdc in
3 +Vdc out
4 Common out
5 -Vdc out

Order your newly designed A Series converters now. We've shaved cost — not quality. That's why SCI is the No. 1 SOURCE

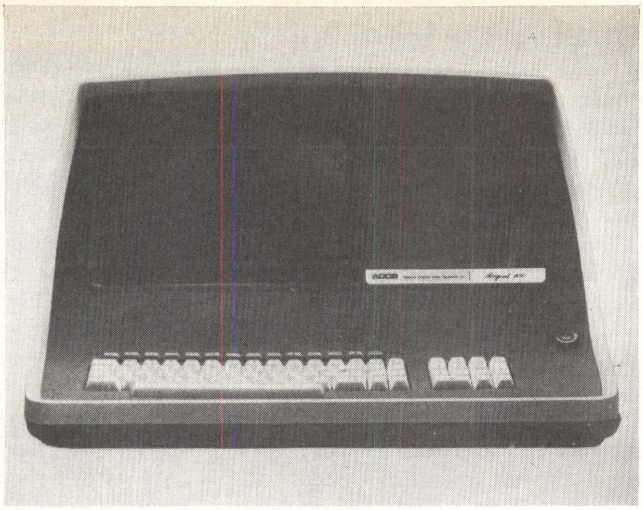
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PRODUCTS

Teletypewriter-Compatible CRT Terminals Cover Wide Range of Data Entry Requirements

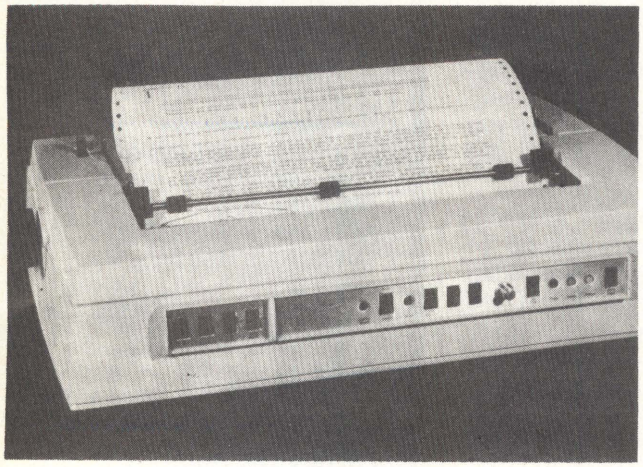
Both Regent 100, a teletypewriter replacement, and Regent 200, for users with sophisticated data entry requirements, feature full 128-char ASCII keyboard, u/lc characters in 8 x 8 dot matrix, separate 14-key numeric pad, 11 special graphics symbols for line drawing capability, and 24-line x 80-char page display in dark characters on light background. A status line at the bottom of the screen, distinct from the page display, shows the terminal's operating status or the results of a self-diagnostic test of memory and communications interface. Information can be highlighted by using reverse video, underlining, half intensity, and blinking. The 100 is a conversational terminal, with char-at-a-time transmission, while the 200 provides two buffered transmission modes and a powerful formatting capability. Screen size is 12″ (30.5



cm) diag. Refresh rate is 60 frames/s (50 frames/s for export models). Transmission is switch-selectable half- or full-duplex. **Applied Digital Data Systems,** 100 Marcus Blvd, Hauppauge, NY 11787.

Circle 200 on Inquiry Card

Byte-Format Daisywheel Printers Read Both Serial and Parallel Data



Because they are based on a single-byte/character organization and can read both serial and parallel data, Sprint Micro 5 family printers plug directly into the I/O channels of any size CPU without special interfacing or software. In byte mode a set of 58 commands defines format and character spacing for the entire text to be printed, without need for the usual extra control byte required by conventional daisywheel printers. The data system can also specify such variables as hammer intensity, ribbon color, vertical and horizontal tabs, and operating mode, including normal, program, or graphics. Keys to these capabilities are a single-chip microprocessor and an expanded command set. An 8-bit std ASCII parallel interface connects the printer to a CPU or other source of 7-bit ASCII characters; an optional RS-232-C interface enables remote terminal communications. Buffers permit simultaneous parallel and serial data reception from two sources. **Qume Corp,** 2323 Industrial Pkwy W, Hayward, CA 94545.

Circle 201 on Inquiry Card

Portable Device is High Speed Program Loader for Computers, Controllers, Terminals, Data Sets

Intelligent interfacing for STR®-Link II, a complete storage system including drive, electronics, power supply, and serial interface in a briefcase, is provided by a 6800 microprocessor. Low cost digital cassettes are used as the storage medium, and manual or remote control can be used for record/playback of serial data. Control of standard RS-232 functions can be done via handshake lines or with control characters in the data stream. The device provides permanent storage and playback of digital information such as diagnostic routines and computer programs, and can be used as a transparent storage medium in serial interfaces (RS-232, 20-mA current loops), and paper tape replacement in applications such as TTYs. Dual RAM buffer enables read and write operations at different speeds, while an optional buffer allows incremental operation, data compaction, a peak rate of 9600 baud, and variable record length. **Electronic Processors, Inc,** 1265 W Dartmouth Ave, Englewood, CO 80110.

Circle 202 on Inquiry Card



Anode lead wire for impressed current anodes for use in deep ground beds, sea water and other severe cathodic protection environments.

Jackets for use as cladding over glass fiber bundles in transportation applications utilizing fiber optics.

Electrical heat tracing systems maintain process temperatures in liquid-handling systems (pipes, valves and fittings). Also used to freeze-protect pipes under extreme climatic conditions.

Heat shrinkable tubing protects critical diodes and capacitors, carbon deposited resistors and provides support for butt-welded connections.

Solder Sleeves® provide electrical solder connections for wires, cables, cable shields and coaxial cables.

Insulated terminals for nuclear power plant, aircraft, aerospace and pipeline installations.

Cable ties for nuclear and other tough environmental applications.

Jacket cable constructions for aerospace, electrical and electronic systems, airframe wiring, outerspace environments, high density wiring and other complex circuitry.

KYNAR® Resin protects your wiring system end to end.

It's the unique balance of these properties that enables KYNAR to perform in many tough applications:

Kynar can be marked, printed, striped, or hot stamped for identification. It can also be pigmented for color coding.

Kynar has high dielectric strength and good insulation resistance.

Kynar has a temperature range from −80° to +300°F.

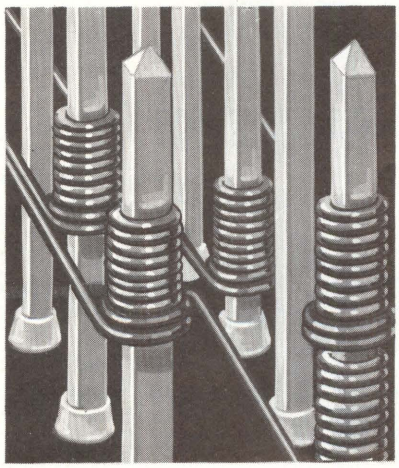
Kynar is nondripping, self-extinguishing (UL STD 94 V-0) and has an LOI (Limiting Oxygen Index) of 45.

Kynar has good chemical resistance, low permeability.

Kynar has a tensile strength of 7000 psi. It is mechanically strong and has good abrasion and cut-through resistance.

Kynar has low-moisture absorption (0.04%), excellent radiation and UV resistance.

For list of fabricators, more technical data, specifications (UL and military), write or call Joe Michaud. Plastics Department, Pennwalt Corporation, Three Parkway, Philadelphia, PA 19102. (215) 587-7520.



Kynar insulated wire is ideal for automatic wire wrapping operations for computer back panels.

*KYNAR is Pennwalt's registered trademark for its polyvinylidene fluoride resin.
®Solder Sleeves is a registered trademark of Raychem Corporation.

PENNWALT
CHEMICALS ■ EQUIPMENT
HEALTH PRODUCTS

CIRCLE 78 ON INQUIRY CARD

FINALLY!



I can easily interface my minicomputer system to the 360/370.

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Want more information about the 8500? Call or write, today.

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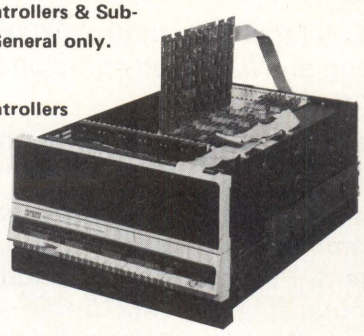
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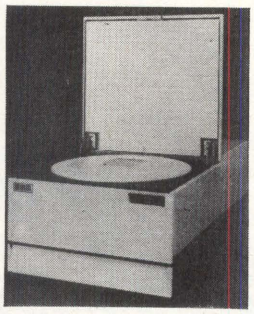
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CIRCLE 80 ON INQUIRY CARD

PRODUCTS

COMBINATION MEDIA DISC STORAGE SYSTEM



Capacities of 25M, 50M, and 76M bytes of fixed and removable storage are available on the model 312 system. Multiple units can attain a capacity of up to 305M bytes. Data transfer rate is 5 MHz, and average access time is 35 ms. The system is a self-contained random-access storage unit with power supply, logic chassis, and integral clean air mechanism. Options exist for the use of two or three fixed discs plus a removable disc cartridge. The fixed portion of the disc requires only one dedicated servo surface and only one surface of the cartridge for servo writing. All operator controls are on the front panel. The system is available in rack mount or desktop configurations. **EMM Peripheral Products Div,** 1015 Timothy Dr, San Jose, CA 95133.

Circle 203 on Inquiry Card

INTELLIGENT TIME DIVISION MULTIPLEXER

Microprocessor-controlled Timeline 780 Supermux TDMs continuously monitor and report on network status; a teleprinter or ASCII-compatible hardcopy or CRT terminal at the central site reports on the entire system. Units can double the throughput of conventional multiplexers since they transmit only actual information without wasting bandwidth on idle lines. An ARQ technique eliminates transmission errors. Data are temporarily stored, checked for errors, and if necessary, retransmitted. Any mix of synchronous and asynchronous, dial-up, and dedicated inputs to 9600 bits/s can be accommodated. Up to 128 inputs may be multiplexed over a single output line. **Infotron Systems Corp,** 7300 N Crescent Blvd, Pennsauken, NJ 08110.

Circle 204 on Inquiry Card

LABORATORY/SCIENTIFIC COMPUTER SYSTEMS



Two computer systems suited for scientific uses contain all necessary hardware, software, and services. LS-16 includes 16-bit model 5/16 processor with 48k bytes of mainframe memory, dual floppy disc drive, CRT terminal, 16-channel ADC, OS/16 MT2 foreground/background operating system, and extended FORTRAN IV. FPS (FORTRAN Processing System), the second system, includes a 32-bit model 8/32 Megamini^R processor with 256k bytes of memory, floating-point hardware, bootstrap loader, 10k bytes of disc storage, CRT terminal, OS/32 MT multitasking operating system, and FORTRAN VI (ANSI FORTRAN compiler). **Interdata, Inc, a unit of Perkin-Elmer Data Systems,** 2 Crescent Rd, Oceanport, NJ 07757.

Circle 205 on Inquiry Card

AUTOMATIC SEND-RECEIVE PORTABLE DATA TERMINAL



Integral RAM and mini-cassette tape operating in tandem provide the Miniterm 1205 with simultaneous transmit and receive capability; tape-to-memory, memory-to-tape, and either tape- or memory-to-line transmission; and complete editing capability for offline data or report preparation. Built-in modem and acoustic coupler are compatible with timesharing systems and central computers over telephone lines. RAM is expandable from 8k to 32k 8-bit char. Print speed is 35 char/s. Mini-cassette stores 68k char; line buffer holds 1000 char. **Computer Devices Inc,** 25 North Ave, Burlington, MA 01803.

Circle 206 on Inquiry Card

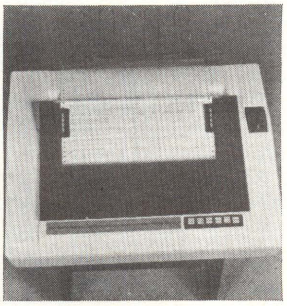
NUMERICAL CONTROL UNIT PLUG-IN PROGRAM MEMORY

SAM (standalone memory) plugs into most machine tools to functionally bypass tapes and tape readers. It stores 8k char (equal to >60 ft of punched tape) and operates at up to 1k char/s (compared to 50 to 300 char/s for tape readers). Since it instantaneously returns to the beginning of a part program after a cycle, the wasted time for tape rewind is eliminated. An interface allows the memory to respond like the computer memory of a CNC. Any part program can be dumped into SAM directly from the memory of a program tape editor, or it can be loaded from a portable reader at 300 char/s. **Alden Self-Transit Systems Corp,** 2 Mercer Rd, Natick, MA 01760.

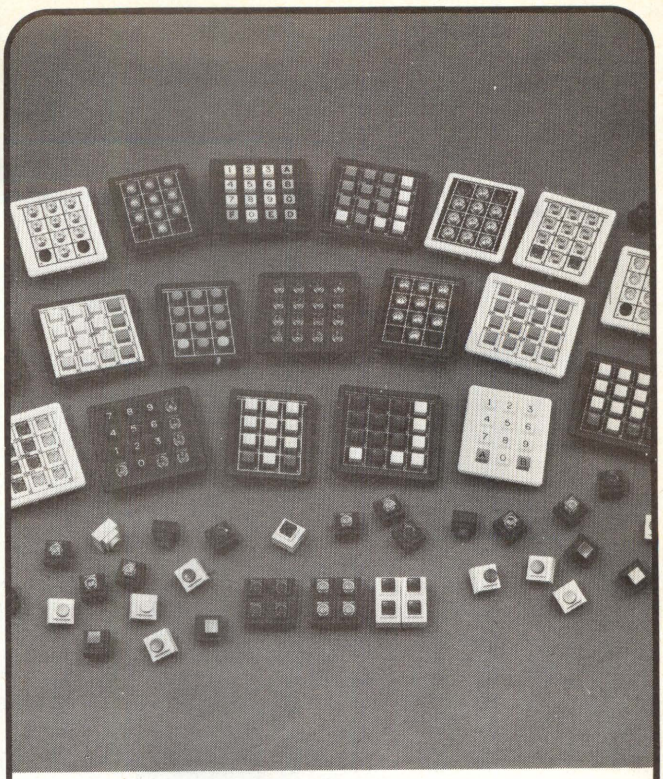
Circle 207 on Inquiry Card

INTELLIGENT PRINTER SYSTEM

A 120-char/s, bidirectional dot matrix printer, combined with an 8-bit microcomputer in the model 7000 system, uses only 25% of the available processing power (1k words of RAM and 2k words of p/ROM). Up to 3k RAM and 4k p/ROM are available for other user applications. The microcomputer includes eight input registers, up to six of which are available to users, and eight output registers, three of which are available. A built-in diagnostic package permits 100% offline system testing. Parallel interface is std. **Dataroyal, Inc,** 235 Main Dunstable Rd, Nashua, NH 03060.



Circle 208 on Inquiry Card



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- Burroughs,

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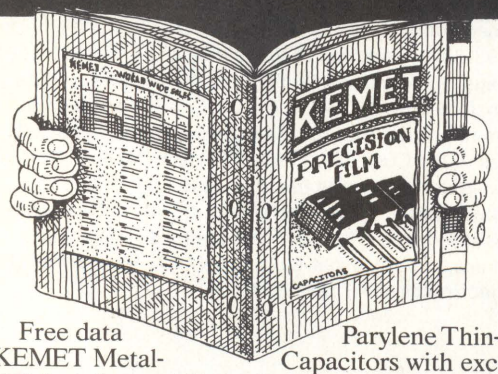
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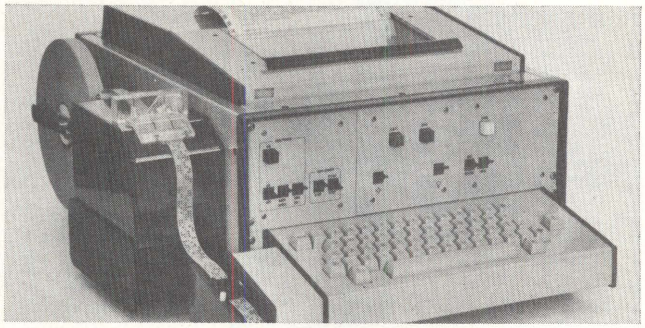
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PRODUCTS

MULTILANGUAGE AUTOMATIC SEND-RECEIVE TELEPRINTER



Capabilities of the BT-3502 include transmission and reception of messages in all horizontally-written languages, reading either left to right or right to left. Dot matrix formation (7 x 13) enables construction of both letters and symbols, permitting any language to be programmed. Baudot-coded information may be input from either keyboard or paper tape reader, and output as both hardcopy and punched paper tape. Transmission-reception rate is selectable at 50, 75, or 100 baud by internal strapping. (Rates up to 20 char/s are also available.) Power requirements are 115/230 Vac ±10%, 50-60 Hz, single phase. **Solcoor Inc,** 415 Madison Ave, New York, NY 10017.

Circle 209 on Inquiry Card

µP HARDWARE/SOFTWARE LOGIC ANALYZER



Model 50D16, a 16-channel, 50-MHz instrument, is intended for microprocessor system designers who must debug both hardware and software. A data trigger mode allows the user to insert up to three sample bits of delay in the trigger, which eliminates unwanted triggering on static or noise. A 3-digit control panel LED display reads in sample bits, the distance between the trigger marker, and the adjustable cursor. This simplifies timing analysis by eliminating the need for look-up tables or additional equipment. The analyzer weighs 18 lb (8.2 kg) and measures 6.75 x 8.5 x 14" (17.15 x 21.6 x 35.6 cm). **BP Instruments, Inc,** 10601 S De Anza Blvd, Cupertino, CA 95014.

Circle 210 on Inquiry Card

DOUBLE-SIDED, DOUBLE-DENSITY FLEXIBLE DISC DRIVES

Model 9406 provides a maximum unformatted storage capacity of 1.6M bytes on an IBM Diskette 2 or compatible storage media; microprocessor-controlled 9474, which incorporates one or more double-density, double-sided drives, provides up to 6.4M bytes of unformatted data storage capacity in a 4-drive configuration. The 9406 operates with data formatting and timings resident in the host controller. Single- or double-density media are interchangeable with that used on IBM System 32 and 34 drives, and on IBM 3740 terminal equipment. In the 9474 an Intel 8080 controls track selection, head loading, data format recognition, and generation. **Control Data Corp,** Box O, Minneapolis, MN 55440.

Circle 211 on Inquiry Card

CIRCLE 83 ON INQUIRY CARD

WRIST CALCULATOR/WATCH/ALARM



Resembling a digital watch, the 6-oz HP-01 combines six interactive functions: time, alarm, timer/stopwatch, date/calendar, calculator, and memory. 28 keys (six finger-operated, 22 stylus-operated) are used in operation. There are 12 different display modes or indicators. Time is shown in hours, minutes, and seconds with one push of a key. A 2.5-s beeping alarm can be set up to 24 h ahead of time, while a second alarm can be set to count down from a preset time. The timer/stopwatch displays elapsed time in hours, minutes, and seconds or minutes, seconds, and hundredths of seconds. A 200-yr calendar displays the date in either the month, day, year or day, month, year formats. **Hewlett-Packard,** 1501 Page Mill Rd, Palo Alto, CA 94304.

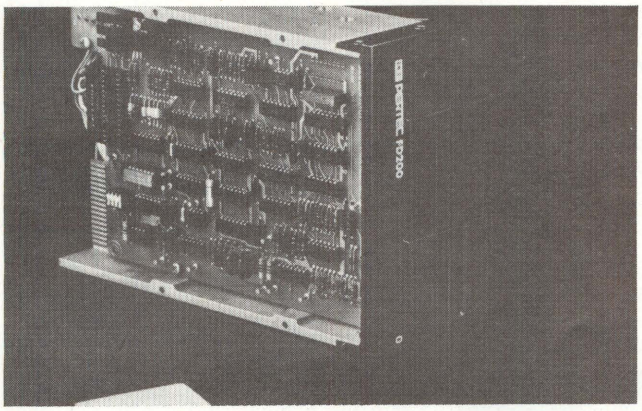
Circle 213 on Inquiry Card

NON-VOLATILE SEMICONDUCTOR MEMORY

A RAM module for mini and microcomputer systems, the in-8100 stores 4k bytes of data and retains those data for a minimum of 96 h after system power supply failure or shutdown. Each module contains resident standby power supply consisting of battery charger, flat Ni-Cad battery, and an interface that senses loss of system power and puts the memory on standby power. In normal operation, module draws only 1.7-A max current from a single 5-V power supply. Data are stored in an array of 5101 CMOS static RAMs. Basic card operates in two jumper-selectable modes: 2048 words by 16 bits or 4096 words by 8 bits. TTL-compatible bus interface provides 16 bidirectional data I/O lines, 16 address inputs, and control lines. **Intel Memory Systems,** 1302 N Mathilda Ave, Sunnyvale, CA 94086.

Circle 214 on Inquiry Card

DOUBLE-DENSITY, DOUBLE-SIDED SMALL-FLOPPY DRIVE



Double-density recording of 250k bytes on each side of a 5.25" (13.34-cm) diskette is offered by the model FD200 Microfloppy™. It is mechanically and functionally interchangeable with Shugart drives but permits writing on 40 tracks vs a 35-track limit for the SA400. Both signal interface connector and dc power connector are compatible with Shugart equipment, and mounting holes and outline dimensions are the same. Up to four drives can be daisy-chained on a single 34-line ribbon cable. Interface electronics are reduced to a single IC circuit board. The drive uses an IBM-compatible read/write head with "tunnel erase." Recording density at the inside track is 2581 bits/in. **PCC/Pertec,** 21111 Erwin St, Woodland Hills, CA 91367.

Circle 215 on Inquiry Card

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(Computer Hardware & Software)

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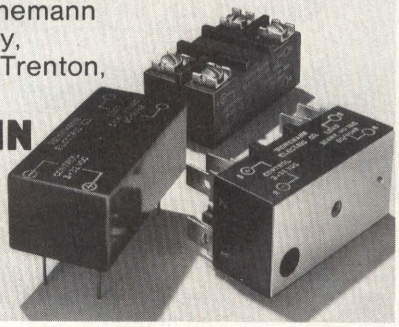
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Call (609-882-4800) or write for further information. Heinemann Electric Company, Brunswick Pike, Trenton, NJ 08602.



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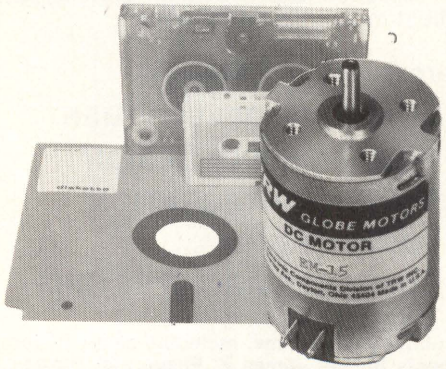
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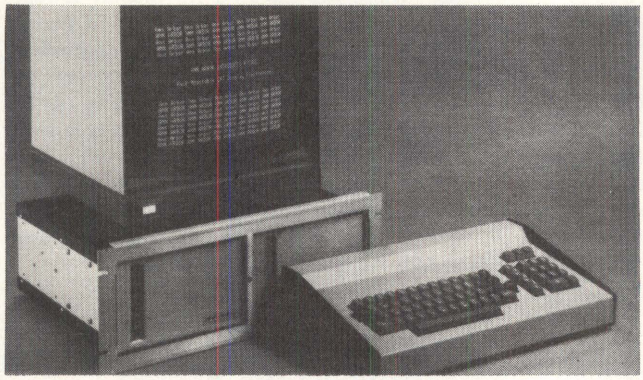
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PRODUCTS

RACK-MOUNTABLE CRT DISPLAY CONTROLLERS



Basic rack-mountable terminal systems for OEM and industrial uses include timing, memory, cursor, serial KSR boards as appropriate, and power supply. R-case units are available in alphanumeric display formats ranging from 8 lines of 32 char to 24 lines of 80 char, and can drive single or multiple arrangements of RS170 video monitors. Configurations include single unit, two units bolted together, and rack-mounting in single or dual configuration. A multidrop option allows up to 64 displays to be remotely addressed and written over a single communications line. **Ann Arbor Terminals, Inc,** 6107 Jackson Rd, Ann Arbor, MI 48103.

Circle 216 on Inquiry Card

50M-BYTE DISC CARTRIDGE DRIVE

Front-loading M2201 stores 50M bytes of unformatted data on two discs within a cartridge. The single actuator is a linear motor employing a track-following servo system. A std storage module interface enables the drive to be added to an existing disc configuration. Formatted capacity is 39.7M bytes. Transfer rate is 6.55M bits/s (819k bytes/s). Avg access time is 30 ns. Power requirements are 115 V ±10%, 60 Hz +1% −3%, 1.3 A max operating; 5 Vdc at 5 A, 12 Vdc at 1.5 A, −12 Vdc at 1.5 A, and −32 V at 6.5 A. Ambient operating temperature range is 41 to 104°F (5 to 40°C), 20 to 80% RH. **Fujitsu America, Inc,** 2945 Oakmead Village Court, Santa Clara, CA 95051.

Circle 217 on Inquiry Card

500-TERMINAL CAPACITY NETWORK PROCESSOR



Up to 250 simultaneous "conversations" with 32k char/s total throughput can be handled by Dynaplexer with the company's T-4, -16, -20, and -96 TDM families. Traffic is removed from TDM channels which carry no useful information and the remaining data are averaged. Compaction may be performed on all types of asynchronous TDM channels as well as synchronous channels using a BSC format. Speed/code intelligence at the computer front end is eliminated by determining the terminal's speed/code and connecting it to any available port in that speed/code group. Other features include automatic rerouting in the event of a link failure. **Timeplex, Inc,** 100 Commerce Way, Hackensack, NJ 07601.

Circle 218 on Inquiry Card

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Everyone that's interested in Telecommunications is headed for Georgia October 9th to 15th. Why are they going to Georgia? To attend the first International Telecommunications Exposition to be held in the United States. INTELCOM 77 will be held October 9th to 15th and will include Technical Programs, Financial Seminars, Applications, "Mini Telecommunications University" Courses and 250 of the world's largest exhibitors that will show the most up-to-date equipment in the world today. . .along with live demonstrations to show you how it works. All segments of the Telecommunications Industry worldwide will be there. You'll hear Experts Analyze Today's and Tomorrow's Trends in Computers and Telecommunications technology, and you'll See What's Available today and What's Coming Tomorrow . . .all in one short week in Atlanta, Georgia, October 9th to 15th.

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PRODUCTS

UNIVERSAL PRODUCT CODE HAND-HELD WAND SCANNER

In addition to slot-type scanners for maximum checkout speeds, food stores now have greater flexibility available with hand-held scanners. For use in such areas as the store's courtesy booth, checkout lanes, and back-office areas, the 7877 UPC hand-held wand scanner complements the company's current "slot" scanner mounted in checkout stands. Both scanners can be used with the company's 255 computerized checkout system. **NCR Corp,** Dayton, OH 45479.

Circle 219 on Inquiry Card

2-OF-5 BAR CODE READER



The V11010 bar code reader is available as a complete code reading system or as any combination of its components. It utilizes an optical scanner to detect the change in reflected light between the bars. A current directly proportional to the amount of reflected light is produced, amplified, and converted to a square wave voltage signal. The device offers a choice of optical scanners, signal conditioners, and outputs. Either a series of hand-held incandescent or LED version code pens, or fixed position, coaxial reflective scanners can be used to read codes. **Skan-A-Matic Corp,** PO Box S, Elbridge, NY 13060.

Circle 220 on Inquiry Card

DIP OPTO-ISOLATOR

The P1063 device with GaAs-LED and silicon phototransistor has a fast rise time of 2.0 μs typ. Complete electrical isolation is maintained between input and output. Circuit coupling of HNIL with TTL is optical, allowing 1500-Vac isolation between input and output. Applications for the device include I/O interface for computer, interface between isolated circuits, and solid-state switches. **Hamamatsu Corp,** 120 Wood Ave, Middlesex, NJ 08846.

Circle 221 on Inquiry Card

SELECTRIC-BASED COMPUTER TERMINAL



In std configurations, the terminal enters and receives ASCII data synchronously at up to 300 baud and is plug-compatible with the serial I/O port of most calculators. The microprocessor-based system operates with acoustical couplers and modems via the RS-232 interface. Fully buffered, with switch selectable transmission rates of 110, 134.5, 150, and 300 baud, the terminal has a printing capacity of 15 char/s. **CPT Corp,** 1001 S 2nd St, Hopkins, MN 55343.

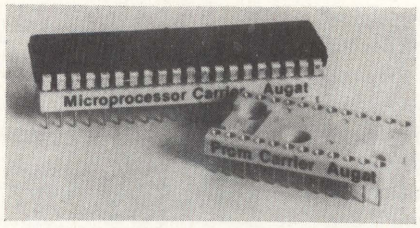
Circle 222 on Inquiry Card

POLAR-TO-CARTESIAN COORDINATE CONVERTER

Providing the means of displaying polar coordinate display information on a std X-Y display oscilloscope or plotter, model 5090 accepts angle and radius inputs, and furnishes vertical and horizontal, or X and Y coordinate output information. Operating trigonometric range is ±180 deg and typical accuracy is ±0.5%. Unit features ±10 V input and output levels, dc to 10-kHz min trig function large signal bandwidth, and dc to 300-kHz small signal. **Optical Electronics Inc,** PO Box 11140, Tucson, AZ 85734.

Circle 223 on Inquiry Card

µP and p/ROM CARRIERS



Protecting leads of 40-pin microprocessors or 24-pin p/ROMs, the carriers hold the devices and plug into any IC socket or packaging panel. The two carriers have 0.018", ±0.003" (0.046, ±0.008 cm) diameter pins of phosphor-bronze base material to withstand a high number of insertions and withdrawals. Gold-plated contacts feature closed-end construction to eliminate solder flux or wicking problems. Carriers meet most severe environmental conditions. **Augat Interconnection Products, a div of Augat Inc,** 33 Perry Ave, PO Box 779, Attleboro, MA 02703.

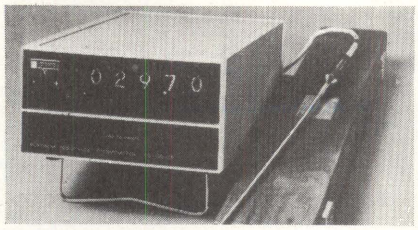
Circle 224 on Inquiry Card

DPM BCD-TO-TELEPRINTER CONVERTER

Digital panel meter BCD outputs are converted to Teletype™ inputs for hard copy and paper tape with the model DPT-415. Running on a 5-V power supply, it has a preset format for printing meter readings up to five digits, a sign, and an additional character. It generates spaces, carriage returns, and line feeds. Driving circuitry for a 20-mA Teletype connection is included on the 6.5 x 4.5" (16.51 x 11.43 cm) circuit board. **Digital Laboratories,** 600 Pleasant St, Watertown, MA 02172.

Circle 225 on Inquiry Card

DIGITAL TEMPERATURE STANDARDS

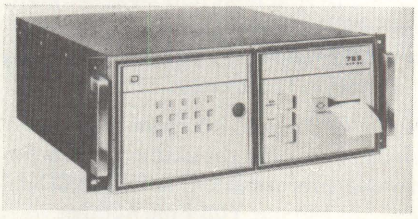


Temperature measurement standards are available in three complete systems, each consisting of a calibrated platinum resistance temp detector probe and a drift-free digital indicator calibrated to match probe characteristics. Secondary standards system (DS-100-T5A-1330) has calibration accuracy of ±0.1°C over a −100 to 200°C range. Portable industrial grade system (410A-5042) has a calibration accuracy of ±0.3°C. **Doric Scientific Div, Emerson Electric Co,** 3883 Ruffin Rd, San Diego, CA 92123.

Circle 226 on Inquiry Card

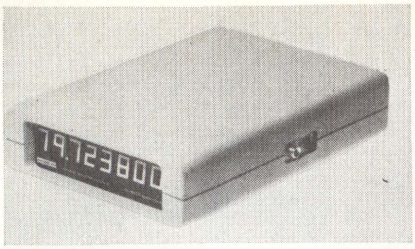
2400-LINE/MIN SERIAL PRINTER

Model 722-247G is designed for high speed impact printing at high baud rates. Print speeds are up to 2400 lines/min or 52,800 char/min for numeric printers, and 13,200 char/s for alphanumeric ASCII printers. Standard interfaces are for either RS-232-C or 2-mA loop. The unit measures std 19" (48.26 cm) rack or table 7 x 18" (24.78 x 45.72 cm). Weight is 75 lb (33.77 kg). **Datadyne Corp,** PO Box 247, King of Prussia, PA 19406.



Circle 227 on Inquiry Card

20-HZ TO 100-MHZ FREQUENCY COUNTER



Providing accurate frequency readings from 20 Hz to 100 MHz for audio, ultrasonic, rf (am and fm), video, and digital applications, MAX-100 solid-state frequency counter requires only a clip-lead or other input cable, or mini-whip antenna in order to operate. It automatically gives direct frequency readings on an 8-digit, 0.6" (1.524-cm) LED display. Readout is updated once a second; overflow signals (above 100 MHz) are automatically indicated. Unit operates on six AA cells, 110 or 220 Vac, 12 Vdc, or any 7.2- to 10-Vdc supply. **Continental Specialties Corp,** 44 Kendall St, PO Box 1942, New Haven, CT 06509.

Circle 228 on Inquiry Card

µP-BASED PLOTTER CONTROLLER

The MPC-11 plotter controller for off-loading plotter software from a host system to a controller frees memory in the host, increases system throughput, and allows user-choice of many incremental plotters. The unit provides the interface, which is either RS-232-C or 8-bit parallel, switch-selectable from 75 to 9600 baud. Features include a char set with special symbols which can be generated, rotated, and scaled by the device; and the ability to clip all portions of a plot outside the boundaries of a user-defined window. **Logic Sciences, Inc,** 6440 Hillcroft, Suite 412, Houston, TX 77081.

Circle 229 on Inquiry Card

CHARACTER-ORIENTED CONVERTER-BUFFER

Operating in full-duplex, half-duplex, or simplex mode on 2- or 4-wire lines as required by the modems, the MPB-200C converter/buffer accepts machine- or hand-keyed data in conventional non-synchronous character format at rates compatible with the high speed modems. It buffers and synchronizes these data with the modem clock. Synchronous data from the modem receiver are accepted and delivered to the terminal or computer in the original character format, but at the higher data rate. **Syntech Corp,** 11810 Parklawn Dr, Rockville, MD 20852.

Circle 230 on Inquiry Card



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PRODUCTS

INTELLIGENT DUAL FLOPPY DISC SYSTEMS



Micro-Flop 11 (MF-11) dual floppy disc system, available with or without a built-in LSI-11, is housed in a 10.5" (26.67-cm) enclosure which holds two floppy disc drives with controller, power supply, slides for rack mounting, and the DEC H9270 backpanel. The controller/interface card provides total software and media compatibility between the LSI-11 and the dual floppy disc system. It can be used with any of the PDP-11V03 software packages. **Charles River Data Systems, Inc,** 235 Bear Hill Rd, Waltham, MA 02154.
Circle 231 on Inquiry Card

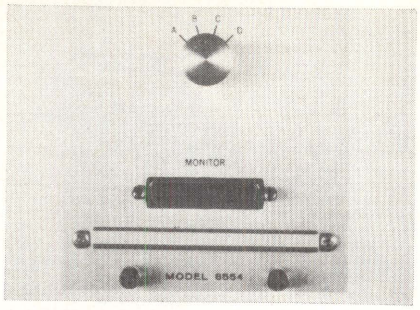
REMOTE LINE PRINTER INTERFACE

MPC-9 provides user flexibility in choice of printers. Using 8080 microprocessor logic, and operating in a synchronous or asynchronous environment, the interface furnishes up to 2k p/ROM, and 1 or 2k RAM which permits emulation of different terminals for print-only applications in multi-drop or switched-line use. It is RS-232-C compatible and operates at >9600 baud. Output is 8-bit parallel, TTL levels, 40 mA. **Air Land Systems Co,** 2820 Dorr Ave, Fairfax, VA 22030.
Circle 232 on Inquiry Card

FLAT CABLE MINIATURE-RIBBON I/O CONNECTOR SYSTEM

Delta Ribbon connectors use "Scotchflex" mass-termination technology for rapid connection to "Scotchflex" flat cable. Typ connection time for the 50-contact connector is ≤30 s. Bail- and screw-mount versions, strain relief clips, and junction shell accessories are available. In addition to data processing I/O, the system is suitable for industrial and telecommunications applications. **3M Co,** PO Box 3360, St Paul, MN 55133.
Circle 233 on Inquiry Card

SELECTOR SWITCH AND MONITOR MODULE



Allowing the user to select any one of four 25-wire EIA RS-232 digital interfaces, model 8554 has a front panel quick connect/disconnect 25-pin connector for monitoring the interface. A 4-position rotary switch on the front panel instantly switches all EIA signals (except frame ground) from the rear panel male connector to one of four female connectors labeled A, B, C, or D. A front panel monitor connector permits the signal to be analyzed by the Hawk 4000 Datatrap. **International Data Sciences, Inc,** 100 Nashua St, Providence, RI 02904.
Circle 234 on Inquiry Card

900-LINE/MIN DRUM PRINTER

Extending the print speed range of the System 1200, model 2442 prints a 64-char set at 900 lines/min. A 96-char set is optional. Features are slewing speeds of 30 in (76.2 cm)/s, and line advance speed of 20 ms. Also included are servo-controlled paper and ribbon feed mechanisms, and a drum gate which swings open to facilitate forms loading and ribbon changes. The 45 x 33 x 26" (114.3 x 83.82 x 66.04 cm) unit uses 1- to 6-part forms. It weighs 420 lb (189 kg). **Mohawk Data Sciences Corp,** 1599 Littleton Rd, Parsippany, NJ 07054.
Circle 235 on Inquiry Card

HEAD-PER-TRACK DISC MEMORY SYSTEM

Complete with daisy chain capability to 2M bytes, expandable to 32M bytes, the System-70 is standard 19" (48.26-cm) rack mountable with field selectable spare tracks. It has avg access time of 8.3 ms, transfer rate up to 512k words/s, and nom rotational speed of 3600 r/min. Features include a dual port controller to two DEC-compatible cables and intercoupler interfaces. 50-Hz operation and up to four series 700 drives per controller are optionally available. **General Instruments Corp, Rotating Memory Products,** 13040 S Cerise Ave, Hawthorne, CA 90250.
Circle 236 on Inquiry Card

Become an Ugly™ Convert.

$5.00 Buys Beautiful Results.

No one wants to lose their figure, that's why we designed the dc-dc converter so you can add 12 and 15 volts without reconfiguring your main supply.

Our new dc-dc converter lets you minimize the number of voltages in your main supply or generate high-efficiency 12 or 15 volt outputs from a battery source.

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CIRCLE 86 ON INQUIRY CARD

ARABIC/FARSI CRT KEYBOARD OPERATING SYSTEM

An optional special program for the Intecolor 8001 data terminal automatically changes the shape of letters depending upon position in a word, allowing operator to enter letters without concern for character form. Arabic, Farsi, or other languages can be entered separately or with English characters. Numerals or English alphabet are automatically justified left. 8001 BASIC language is being made fully compatible to handle all languages. **Intelligent Systems Corp,** 5965 Peachtree Corner E, Norcross, GA 30071.

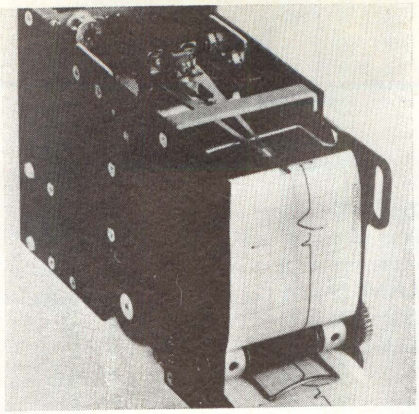
Circle 237 on Inquiry Card

MEMORY MAP ENHANCEMENT FOR CP-V AND -R COMPUTERS

T8215 memory map is supplied as a package consisting of three logic modules, a diagnostic program tape, and a CP-V starter tape. All hardware are mounted inside the CPU cabinet. Memory map can be deactivated or completely isolated from circuitry, and computer is fully compatible with all Sigma 5 software diagnostics. **Telefile Computer Products, Inc,** 17131 Daimler St, Irvine, CA 92714.

Circle 238 on Inquiry Card

MINIATURE STRIP CHART RECORDER



Multiple speed, low power consumption, and performance on either chemical or plastic-coated thermal paper are features of the model M1-40 DCM inkless, thermal writing strip chart recorder. It is designed for the OEM user, with tachometer speed control accuracy of better than 2% and power consumption of 7 W. The device includes up to four chart speeds in 10:1 ratios with the range of 1 to 50 mm/s; it records on a 40-mm wide channel with a front-loading type stylus. It measures 3.8 x 2.5 x 6.5" (9.6 x 6.4 x 16.5 cm) and weighs 40 oz (1.1 kg). **MFE Corp,** Keewaydin Dr, Salem, NH 03079.

Circle 239 on Inquiry Card

14-BIT, 12-μS A-D CONVERTERS

ADC1130 and 1131, a family of high speed, high resolution, 14-bit ADCs, perform conversions in 25 and 12 μs max, respectively. Using successive approximation, both convert analog input voltages into natural or offset binary, and 2's complement coded outputs. Data outputs are provided in parallel and NRZ serial formats. Four analog input ranges—0 to 20, 0 to 10, ±10, and ±5 V—can be user programmed. **Analog Devices, Inc,** PO Box 280, Rt 1 Industrial Pk, Norwood, MA 02062.

Circle 240 on Inquiry Card

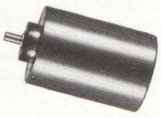
180-DEG VIEWING ANGLE LED

LEDY BUG solves angular dispersion problems through the use of a flat-topped cylindrical lexan fresnel lens. A flat area on the base of the lens denotes the cathode pin. Available in red, amber, or green, the lens is 0.280" (0.711 cm) long and 0.203" (0.515 cm) in diam. It can be mounted on top of or below the panel by clips, bushings, or sockets; with the flat end flush with the panel; or soldered to PC boards. **Data Display Products,** 303 N Oak St, Inglewood, CA 90301.

Circle 241 on Inquiry Card

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35mm of instantaneous power. Featuring long life carbon brushes, ball bearings and our unique hollow rotor to provide you with low noise, high efficiency and coggless performance. Hitachi also makes a full line of ironless core micromotors: 17, 22 and 26 mm diameter series. These motors are precision made with our patented precious metal wire brush system (eliminating brush bounce) Commutators are made of precious metal also, giving maximum life and high reliability for your product. You can't ~~Swiss~~ miss. Special shafts, ball bearings, and modified windings are available to accommodate virtually any specific applications.

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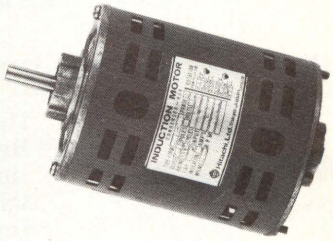
Fractional Horsepower DC Permanent Magnet Motors. (Also available with our incremental encoder complete and assembled.)



Our DC permanent magnet motors have pleased many of our customers in such varied places as printer carriage drives, duplicating machines, x-y axis control drives and high density magnetic tape transports. We can satisfy your application requirements too with one of our various rotor designs or high performance low inertia motors. All are available with our incremental encoder integrally mounted, completely assembled, tested and ready for your immediate installation.

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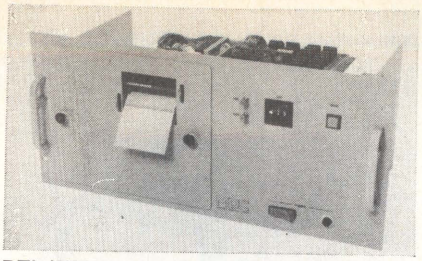
For more information, contact: Hitachi America Ltd., 100 California Street, San Francisco, California 94111. (415) 981-7871 Bill A. Mahoney

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PRODUCTS

RACK-MOUNTED INSTRUMENTATION PRINTER

Ideally suited for use in test equipment, data logging, and power demand monitors, the MDC 316R incorporates a *Precisa* 388 series impact-type printhead with a 12-char/col selection. Characters are printed at a rate of 3 lines/s on std paper rolls or fanfold paper. A parallel BCD interface that is



DTL/TTL-compatible is standard. Options include an integral date/clock, paper-low indicator, and event counter. **Master Digital Corp,** 1308-F Logan Ave, Costa Mesa, CA 92626.
Circle 242 on Inquiry Card

SWITCHING REGULATED POWER SUPPLIES

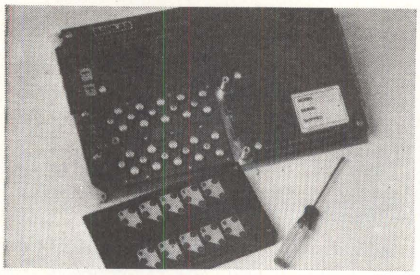
Operating at efficiencies up to 84%, six models from 2 to 28 Vdc with current ratings to 40 A deliver up to 200 W of power from a package measuring 4.75 x 7.69 x 5.03" (12.07 x 19.53 x 12.78 cm) and weighing <5 lb (2.268 kg). All units feature dual wide range inputs, 85 to 132 Vac and 170 to 264 Vac at 47 to 63 Hz, selectable from the front panel. Output regulation is maintained for a minimum of 30 ms after loss of input power to avoid the loss of information in process. Units are rated up to 50°C. **Power/Mate Corp,** 514 S River St, Hackensack, NJ 07601.
Circle 243 on Inquiry Card



TAPE CARTRIDGE DRIVE CONTROLLER

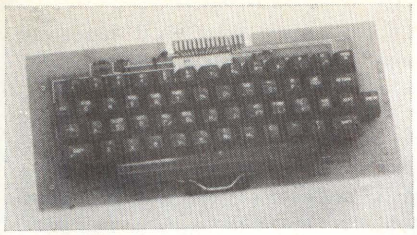
Comprised of a single PCB controller, formatter, and interface, the A 3000 was designed for system integration of the 3M DCD-3 magnetic tape cartridge drive, and S-100 bus structured microprocessor systems. Plug compatible, the unit generates and reads ANSI/ECMA compatible tapes, features a 256- or 1024-byte buffer to free host while performing R/W operations, and has read after write bit-for-bit data verification. Cyclic redundancy check characters are also generated and checked. **Argus Technology Corp,** 7900 Quimby Ave, Canoga Park, CA 91304.
Circle 244 on Inquiry Card

10-CHANNEL THERMOCOUPLE SCANNER



SL102 directly receives grounded, ungrounded, or mixed thermocouples and references, scans, amplifies, filters, and controls the selected signal. AUTO-ICE™ zero stabilizer provides zero referencing for amplifier and on-board reference junction. Other features include a low thermal reed scanner, active 60-Hz filter, and multiplexer for analog output. The control logic is DTL/TTL/CMOS compatible without buffering. **San Diego Instrument Laboratory,** 7969 Engineer Rd, San Diego, CA 92111.
Circle 245 on Inquiry Card

ASCII KEYBOARD



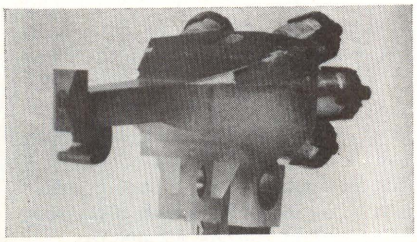
Model 753 keyboard provides ASCII encoding for 53 keys, with the KBM series keyswitches and glass-epoxy PC board assuring mechanical ruggedness and ease of mounting. The interface allows user selection of data and strobe polarity, parity sense, upper-case alpha-lock, and access to three user-definable keys for custom keycode or function key assignment. It is available in either kit or assembled form and comes with documentation. **George Risk Industries, Inc,** GRI Plaza, Kimball, NB 69145.
Circle 246 on Inquiry Card

PDP-8/A & /E SERIAL INTERFACE BOARD

Utilizing one computer slot, the board is a std quad height DEC type with three serial interface connectors attached. Suited to a DEC VT50 or -52, the board is also compatible with std 20 mA teleprinter replacement CRT. Each device is speed selectable in increments from 75 to 9600 baud, and is I/O transfer code selectable as well as word length, parity and stop bit selectable. **Incosan Inc,** 160 Woodport Rd, Sparta, NJ 07871.
Circle 247 on Inquiry Card

9-WIRE DOT MATRIX PRINTHEAD

Model 139 printhead offers 9-wire operation, enabling the user to produce well-defined upper and lower case fonts, and prints many of the symbolic alphabets. It operates with the company's high performance solenoid assemblies, permitting extended duty cycles. Equipped with bearings that accept a 0.5" (1.27-cm) transport shaft, the unit prints a variety of char and graphics at a speed of 110 char/s. Weight is 10 oz (283.49 g). **Victor Comptometer Corp,** 3900 N Rockwell St, Chicago, IL 60616.



Circle 248 on Inquiry Card

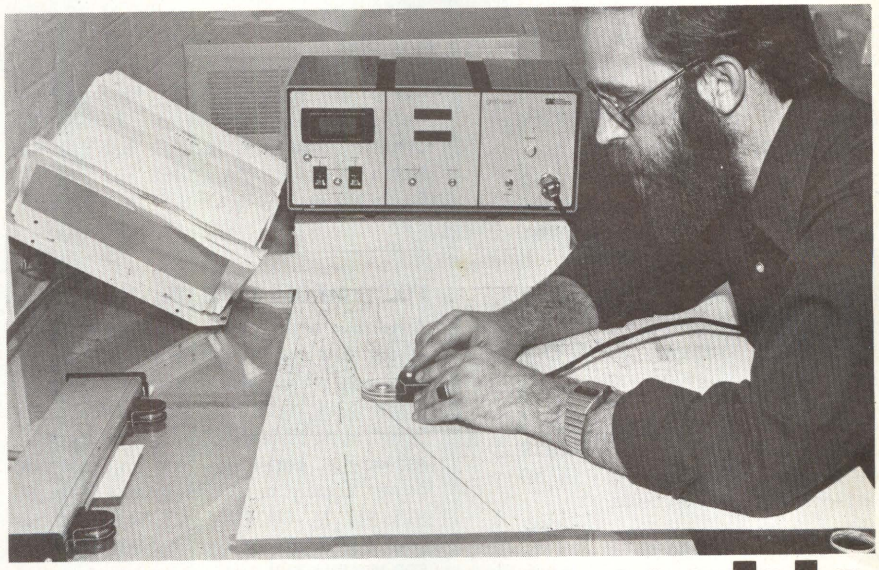
VIDEO DISPLAY PROCESSOR

Comprised of a 16-bit computer, up to 32k words of high speed memory, and a dual floppy disc backup storage, the VDP-1000 is a totally programmable, multi-purpose terminal/processor built around a virtual memory operating system. This affords flexibility in adapting to the user's needs. The operating system is totally transparent and automatically transfers routines and data to/from backup storage. **Lear Siegler Inc, Electronic Instrumentation Div,** 714 N Brookhurst St, Anaheim, CA 92803.
Circle 249 on Inquiry Card

GRAY SCALE SOFTWARE FOR ELECTROSTATIC PLOTTERS

Full gray scale halftones are produced on any of company's electrostatic plotters with Versaplot gray scale software, a universal FORTRAN package. Fine gradations in gray scale with >32 levels of gray are provided, emulated through controlled variation dot clusters on the plotter. The package can modify digital images in outline, spatial frequency, and contour. **Versatec, a Xerox Co,** 2805 Bowers Ave, Santa Clara, CA 95051.
Circle 250 on Inquiry Card

More than a simple sonic digitizer...



our programmable µP-based graphic-to-digital converter.

For those special applications where you want your sonic digitizer to automatically calculate line lengths, areas, volumes, position origins, map coordinate transformations, and other two- or three-dimensional data, we have an exciting new Graf/Pen™ model for you: The NT-501. Our exclusive microprocessor-based programmable sonic digitizer requires only two point sensors above the work area, allowing inter-action with a variety of graphic inputs, such as CRT or plasma displays, projected images, maps, and engineering drawings. And the unencumbered work area provided by the movable point sensors accommodates the use of T-squares, triangles,and other drafting instruments, further facilitating digitization.

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The survey questionnaire is sent only to the precise group of digital design engineers who are qualified to answer your questions. That means no waste and therefore minimum expense.

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COMPUTER-BASED SYSTEMS DESIGNERS	41,075
Business Systems Designers	3,183
Process Monitor/Control Systems Designers	6,002
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You can contact ALL or A SAMPLE PORTION of a particular subcategory.

If you wish more elaborate selections, *they* are available. Suppose you wish to survey *engineering managers* responsible for the *design of disc drives* who influence the *purchase* of *motors*. We can put you in touch with 152 individuals who meet these very special criteria.

Instead of relying on the advice of a limited number of individuals in making design decisions that will impact the market, you can now consult with the entire universe of your prospective clients!

WHAT A WAY TO GO!

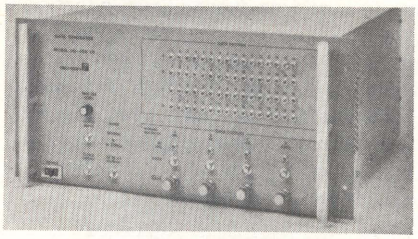
CIRCLE 120 ON INQUIRY CARD

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Dr. Geoffrey Knight, Director
Market Research Group
Computer Design Publishing Corp.
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PRODUCTS

VARIABLE OUTPUT DATA GENERATOR



Model DG-400YH programmable word generator operates from 1 to 400M bits/s and provides a 1-V amplitude, 500-ps rise/fall time signal in NRZ or RZ mode. The unit may be programmed to provide data outputs of four words of 16 bits each, two words of 32 bits, or one word of 64 bits. True and complement data are simultaneously available. RZ or NRZ formats are individually selectable on each data channel. **Tau-tron, Inc,** 11 Esquire Rd, North Billerica, MA 01862.
Circle 251 on Inquiry Card

FIXED MEDIA DISC DRIVES

Available with online capacities of 25, 50, or 100 megabits, the DM-400 series consists of single- and dual-disc versions with 1800- or 2400-r/min rotational speeds, and 100- or 200-track/in recording densities. An internal dc power supply functions from 117 V, 60 Hz; 117 V, 50 Hz, or 230 V, 50 Hz sources. Max power consumption is 500 W. The 5.25" (13.33-cm) high drives weigh 45 lb (20.25 kg) and can be mounted on a std 19" (48.26-cm) EIA rack. **Ampex Corp,** 401 Broadway, Redwood City, CA 94063.
Circle 252 on Inquiry Card

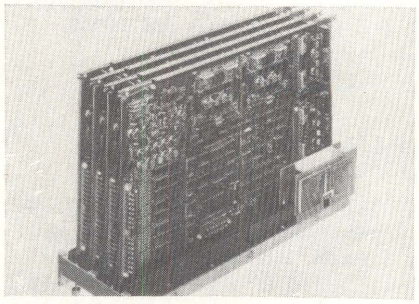
32-BIT INTELLIGENT CABLE I/O INTERFACE

Eliminating the need to design and implement special interface logic, the general-purpose intelligent cable (GPIC) interfaces directly with most low/medium speed devices. Word width is selectable in 8-bit increments to 32-bits. Output data are stored on a full 32-bit buffer which is Picoprocessor-controlled. Data are transferred by a 2-wire strobed or handshake protocol. Automatic or DMA I/O simplifies programming protocol and permits direct to/from memory transfers without program intervention. **Computer Automation, Inc,** 18651 Von Karman, Irvine, CA 92713.
Circle 253 on Inquiry Card

DUAL TONE TOUCH-TONE ENCODER

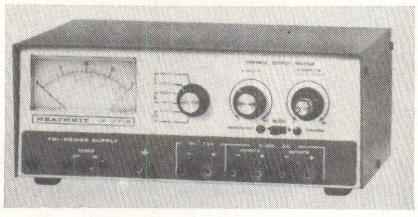
An epoxy encapsulated dual frequency signal generator module capable of producing all 16 tone pairs required for multifrequency Touch-Tone™ dialing, model DTE-100 is designed for telephone and mobile radio communication, and remote control and data acquisition applications. The unit features an internal voltage regulator and ceramic oscillator, requiring no external components. Specs include 900 mV rms adjustable composite output into 600 Ω, and 1.7 dB high frequency preemphasis. **Data Signal Corp,** 40-44 Hunt St, Watertown, MA 02172.
Circle 254 on Inquiry Card

ADD-IN CORE MEMORY



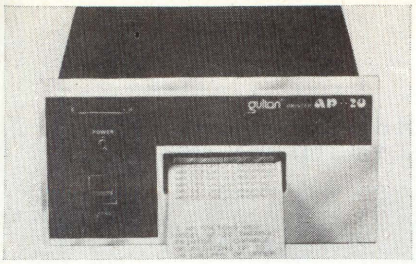
Designated the DR-114, the system is available is 16k x 18 or 32k x 18 configurations and is completely plug-compatible with DEC's MM11-D and -DP single board systems for PDP-11/04 and /34 minicomputers. It has a cycle time of 900 ns and access time of 350 ns. Operating temperature range is 0 to 55°C. Four systems can be combined to provide a maximum capacity of 128k x 18. **Dataram,** Princeton-Hightstown Rd, Cranbury, NJ 08512.
Circle 255 on Inquiry Card

3-OUTPUT POWER SUPPLY FOR EXPERIMENTERS



Available in kit form, the IP-2718 has a single fixed 5-Vdc output at 1.5 A and two variable 0- to 20-Vdc outputs at 0.5 A which can be tracked to follow each other at any specified voltage difference, useful in analog circuits requiring ± voltage. Outputs are short-circuit proof with current limiting. A switch-selectable front panel meter monitors all outputs. **Heath Co,** Dept 350-24, Benton Harbor, MI 49022.
Circle 256 on Inquiry Card

20-COL ALPHANUMERIC THERMAL PRINTER



A self-contained alphanumeric thermal printer with transport, electronics including power supply, controls, and a panel mounting enclosure, model AP-20 utilizes a thick film dot matrix thermal printhead which prints up to 20 col of 5 x 7 dot char at a 2.5-line/s rate. A full upper case 64-char ASCII subset is provided via a character serial, bit parallel interface. Paper tape advances after printing a dot row. Paper advance is accomplished using a permanent magnet dc stepper motor geared to increment the drive roller. **Gulton Industries, Inc, Measurement & Control Systems Div,** East Greenwich, RI 02818.
Circle 257 on Inquiry Card

SOLID-STATE PM MOTOR SPEED CONTROLLERS

Models SC10, 20, 43, 45, and 45H power matching permanent magnet motors and gearmotors are available in ratings from 0.01 to 0.25 hp with single-source supply for the complete variable speed system. Controllers take 115-Vac single-phase input and operate motors for wide continuously adjustable speed ranges at constant torque. Electronic circuitry contains feedback for motor load vs speed regulation, and has line voltage compensation to hold motor speed constant with fluctuating input voltages. **RAE Corp Systems Group,** 5 Eastern Steel Rd, Milford, CT 06460.
Circle 258 on Inquiry Card

ABSOLUTE ENCODERS

A true size 23 synchro mounting optical shaft encoder for land-based, shipboard, or airborne applications. Digisec RA/23(C) series is available in resolutions from 11 to 13 bits of parallel, binary code. It is also available in a geared pair configuration to provide resolutions from 17 through 20 bits in a single word. With a single input voltage of 5 or 6 Vdc, the self-contained module features an operating speed of 360 r/min and a nonoperation slew speed of 3600 r/min max. Operating temp range is —40 to 85°C. **Itek Corp, Measurement Systems Div,** 27 Christina St, Newton, MA 02161.
Circle 259 on Inquiry Card

VOICE TERMINAL DIAGNOSTIC SYSTEM

Allowing immediate field analysis of any fault down to the circuit board level, the T500 is used in combination with company's 4520 interface board. System consists of numeric key pad, alphanumeric display, and cassette tape unit which contains all digital data needed for diagnostic comparisons and provides audio instructions for sequential test steps. Port monitors permit on-line tests. **Threshold Technology, Inc,** PO Box 5332, San Mateo, CA 94404.
Circle 260 on Inquiry Card

DUAL-OUTPUT POWER SUPPLY

HE215 achieves 75% efficiency at full load output with <0.5% mV rms (5 mV pk-pk) typ ripple and noise. User-adjustable dual outputs are from ±12 to ±15 V, 1.5 A each, at 45°C. Input is 90 to 130 Vac (180 to 260 Vac for model HE215E) at 47 to 450 Hz. Minus output tracks plus output within ±0.05%. Regulation is ±0.02% max for ±10% line change, ±0.1% max for no load to full load. **Computer Products, Inc,** PO Box 23849, Ft Lauderdale, FL 33307.
Circle 261 on Inquiry Card

The MINIDRIVE™ for the Mini Cartridge



4" x 3" x 4"/Hi Performance/Lo Power
One Moving Part/Hard Mounted Motor

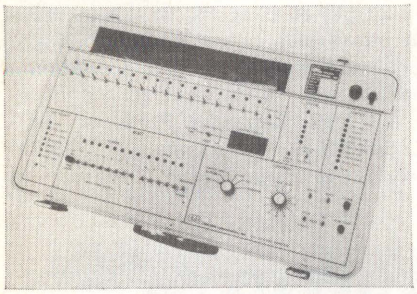
	DENSITY	
	800 bpi	1600 bpi
Tracks	1 or 2	1 or 2
Capacity (bytes) 1 Track	160,000	320,000
2 Tracks	320,000	640,000
Transfer Rate (bits/sec)	24,000	48,000
Speed Read/Write Rewind/Search	30 ips 90 ips	

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- READ-AFTER-WRITE HEAD
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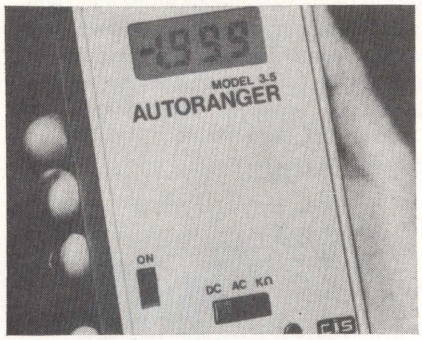
DISC EXERCISER



The portable 20-lb (9-kg) DX-2314 contains such functions as restore, switch seek, seek incrementing, and decrement seek. A seek delay control is provided for alignment adjustments. 16 bits of fixed switch selectable data, 16 bits of incrementing data, and 16 bits of random data are the three basic patterns offered. Drive status indicators are provided to show drive ready, on-line, *unsafe drive*, module select, read only, heads extended, read/write gates, or run. **Wilson Laboratories, Inc,** 2536 E Fender Ave, Fullerton, CA 92631.

Circle 262 on Inquiry Card

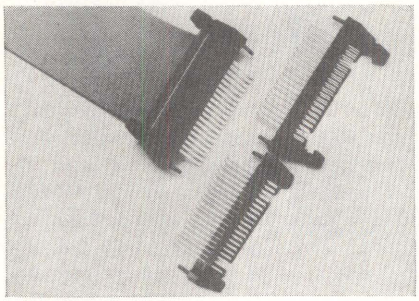
HAND-HELD DIGITAL MULTIMETER



Using low power 3½ digit LCD plus CMOS logic design, Autoranger operates from a single 9-V battery. Features include total automatic operation with autoranging, autozeroing, and automatic lead reversal. The ac/dc voltage to 1000 V and resistance to 1000 kΩ are tested with high accuracy and resolution. Portable high impact case has protected switches. **Control & Information Systems, Inc,** 10 Spring Valley Village, Richardson, TX 75080.

Circle 263 on Inquiry Card

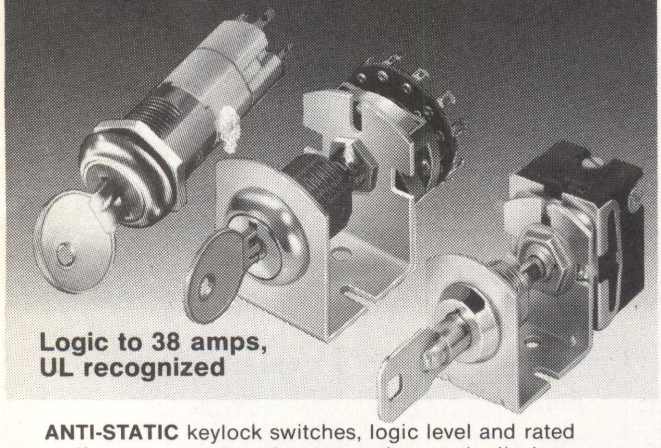
SOLDER AND WRAP TAIL PROTECTED HEADERS



With lock and eject option consisting of dual arms which lock the IDC socket connector firmly in place, and permits rapid disconnect, right angle and straight configuration headers are available with 10, 14, 16, 20, 26, 34, 40, 50, 60, and 64 pins. They mate with std IDC socket connectors on 0.11″ (0.254-cm) grids. Solder tail style has round posts, wirewrap types have square; both are 0.025″ (0.063 cm). **Spectra-Strip, an Eltra Co,** 7100 Lampson Ave, Garden Grove, CA 92642.

Circle 264 on Inquiry Card

Solve your security problems with OAK's complete line of KEYLOCK AND KEY SWITCHES



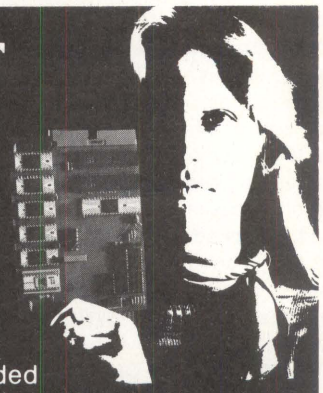
ANTI-STATIC keylock switches, logic level and rated to 4 amps, protect equipment against static discharges to 20,000 volts.

HIGH AND LOW POWER key and keylock switches are available from 2 to 12 positions in almost any switching combination or power requirement.

Many types are stocked by Oak distributors. Call or write for additional information.

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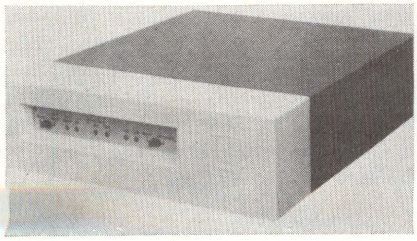
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For a salesman call, circle 93 on Inquiry Card.

CIRCLE 94 ON INQUIRY CARD

1200- AND 2400-BIT/S LSI MODEMS



Operating over 2- and 4-wire leased lines, two LSI modems feature signal loopback capabilities. Model 1200EP, designed for point-to-point and multipoint applications, functions asynchronously up to 1200 bits/s and synchronously at 600 or 1200 bits/s. The CCITT-compatible 2400EP model features 2400-bit/s operation. Both are available in standalone or rackmount configurations. A synchronous remote control plug-in module is optional. **General DataComm Industries, Inc,** 131 Danbury Rd, Wilton, CT 06897.

Circle 265 on Inquiry Card

DATA COMMUNICATIONS TEST PROGRAMS

Intershake[R]-Interview[TM] data communication test system removes test burden from operating system by emulating the host processor. Test program may be run in two modes: automatic, which eliminates need for separate operator, and interactive, used for extensive fault analysis. Each application program operates with both 3271 and 3275 protocols using bisync communications. Highlights include forced error to authenticate error recovery procedures. **Atlantic Research Corp,** 5390 Cherokee Ave, Alexandria, VA 22314.

Circle 266 on Inquiry Card

DESKTOP APL TELEPRINTER TERMINAL

Designed to meet character set requirements of APL users, the 860/A produces both an APL char set with overstrike characters and a high resolution ASCII char set. The unit consists of a 9-wire dot matrix printer mechanism which prints each 9 x 5 char in a 9 x 12 char cell, an ASCII/APL keyboard, and 17 key numeric pad. Std features include speeds of 10, 30, 45, or 60 char/s, horizontal and vertical tabulation, and a 350-char receive-only buffer with overflow protection. **Anderson Jacobson, Inc,** 521 Charcot Ave, San Jose, CA 95131.

Circle 267 on Inquiry Card

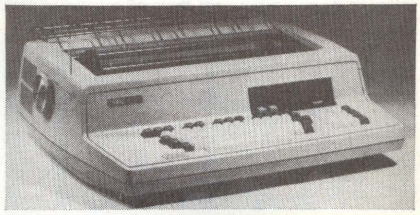
POLLING/ADDRESSING TERMINAL



Burroughs, Lear Siegler, and TEC compatible, the D400 has absolute cursor addressing, field protect format, full text handling edit package, non-glare screen, and u/lc 5 x 9 chars with true descenders. Detachable keyboard generates full 128 ASCII char set and has std alphanumeric typewriter layout with 16 special function keys, 15-key numeric cluster, and 15-key text handling pad. Terminal measurements are 19 x 13.25 x 16.5" (48.26 x 33.65 x 41.91 cm). **EECO,** 1441 E Chestnut Ave, Santa Ana, CA 92701.

Circle 268 on Inquiry Card

SOLID FONT CHARACTER PRINTERS



A family of solid font character printers employ a "thimble" printing element claimed to last 50% longer than many wheel-type elements. The Spinwriter series includes five models, each capable of printing a full 128-char set at up to 55 char/s. The printers incorporate LSI semiconductor technology and are microprocessor controlled. Other features include operation at 60 dB or less with std covers; a choice of five std interfaces, plus custom interfaces; 10- or 12-pitch char printing; and full ASCII code compatibility. **NEC Information Systems, Inc,** 5 Militia Dr, Lexington, MA 02173.

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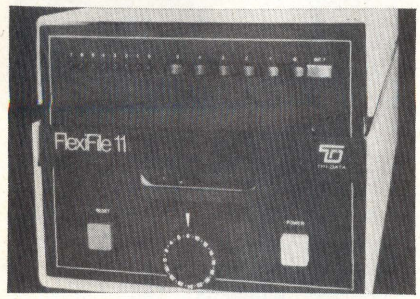
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PRODUCTS

MICROPROCESSOR-CONTROLLED FLEXIBLE DISC SYSTEM

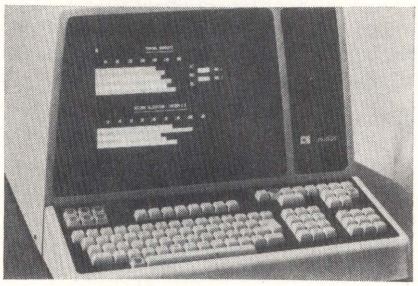


Made up of single- or dual-drives, 8080A microprocessor, and 115-Vac, 60-Hz, 300-W power supply, the FlexiFile 11 is available with optional RS-232 or 8-bit parallel interfaces. Storage capacity is 98k bytes/disc with a transfer rate of 5k bytes/s parallel, 19,200 baud serial. The front panel offers flexibility by means of six mode select switches, and eight indicator lamps which are software defined. **Tri-Data Corp,** 800 Maude Ave, Mountain View, CA 94043.
Circle 270 on Inquiry Card

LINEARIZED DIGITAL THERMOCOUPLE READOUTS

Designed for use with type B, E, J, K, R, S, and T thermocouples, two additions to the Measurometer™ series of digital readouts accurately measure and display temperatures in 14 std ranges from −270 to 1820°C (−454 to 3300°F). PI2466 covers a readout range of −1999 to 1999; PI4466 covers a range of −3999 to 3999. A Thermolizer™ circuit provides max conformity. Polarity sign changes automatically as the reading passes through zero. Both units provide basic readout accuracy of ±0.05% of reading ±1 digit at 25°C. **Analogic,** Audubon Rd, Wakefield, MA 01880.
Circle 271 on Inquiry Card

VIDEO DISPLAY TERMINALS



MIDAS II is a microprocessor-based terminal with eight selectable data transmission rates from 110 to 19,200 baud, and half- or full-duplex mode online operation. Display format of 24 lines by 80 char appears on a 12″ (30.48-cm) diag screen. Features include full 128-char repertoire, solid-state keyboard with numeric pad, and RS-232-C or current loop compatibility. MIDAS III has full keyboard edit, field attribute edit, and 2k-paging option. **Mini-Computer Systems, Inc,** 2258 Via Burton, Anaheim, CA 92086.
Circle 272 on Inquiry Card

GRAPHICS SYSTEM ADD-IN MEMORY

S32K expands Tektronix 4051 memory system from 8k to 32k words of main storage. Plug-compatible, utilizing LSI memory components with all functions transparent, the memory is contained on a 7 x 12″ (17.78 x 30.48 cm) circuit board. All necessary drive and refresh signals are handled on the board with power supplied by the parent computer. Computers with memories of 16k and up can be upgraded with memory expansion kit S8X in 8k-increments, **SDX, Inc,** PO Box 41, Orange Cove, CA 93646.
Circle 273 on Inquiry Card

Hewlett-Packard 9830 Users

You can now dimension, sort and search any array that will fit in your memory.

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CIRCLE 96 ON INQUIRY CARD

REAL TIME SYSTEMS ENGINEERS

The candidates will review, analyze and propose requirements for common real-time system processor communications and peripherals for retail products. They will interact with other corporate and divisional groups for corporate commonality. They will provide consultation to the system/product designer on industry standards interpretation and adherence needs. Generates guidelines on communications and peripherals usage in Retail Systems.
From 3-10 years experience with a BS in Electrical Engineering, Systems Engineering or Computer Science is required; and MS is desirable. Knowledge of one or more of ANSI (ISO) standards on communications cassette, Disk, File formats, peripheral interfaces, code SETS and E.F.T. is very desirable.

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CIRCLE 97 ON INQUIRY CARD

HIGH TORQUE GEARMOTORS

EM-13 gearmotors combine permanent magnet dc commercial motors with a modular, planetary geartrain which provides 30 std speed reduction ratios from 4:1 to 15,625:1. Units feature max continuous torque ranges from 1.5 to 1250 oz-in. Diameter of the motor is 1.25" (3.175 cm); overall length ranges from 3.143 to 4.314" (7.98 to 10.96 cm) depending on the reduction ratio. Devices are built in 6-, 12-, and 24-Vdc models. Life-lubricated bearings and geartrains are std. **TRW Globe Motor Div, TRW, Inc,** 2275 Stanley Ave, Dayton, OH 45404.

Circle 274 on Inquiry Card

NRMA-STANDARD OCR PRINTER

With speeds of 120 to 250 lines/min, units are available with OCR A or B character codes with 132-col print widths. They print 6 lines/in vertical (2.36/cm) and 10 char/in horizontal (3.9/cm) using pin-feed tractors and continuous fanfold paper up to 17.5" (44.45 cm) wide. Printers utilize both RS-232-C communications and standard parallel interfaces. **Data 100 Corp,** 6110 Blue Circle Dr, Minneapolis, MN 55435.

Circle 275 on Inquiry Card

MULTICHANNEL PRINTING EVENT COUNTER

Model 700 combines an electro-mechanical Seico drum printer, digital timer adjustable from 1-99 minute intervals, and eight independent event counters each with a 5-digit capacity. Counters are expandable to 16 channels. Maximum counting speeds are 50,000/s for electrical pulses, and 100/s with debouncing inputs. Separate debouncing inputs enable entry of events from relay contacts or mechanical switches. **Columbus Instruments International Corp,** 950 N Hague Ave, Columbus, OH 43204.

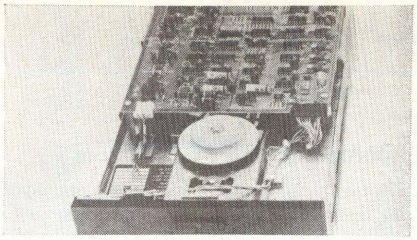
Circle 276 on Inquiry Card

INLINE PACKAGE SOLID-STATE RELAY

Opto-coupled solid-state relay for PC board mounting was designed to provide a 3-A device having a small footprint [(0.4 x 1.7") (1.016 x 4.318 cm)]. Available in 120- or 240-V versions, the relays feature photo isolation, zero voltage turn-on, built-in snubbers, and 2500- or 4000-V rms isolation. Units are suited as microprocessor interfaces for driving motors, solenoids, or lamps. **Opto 22,** 5842 Research Dr, Huntington Beach, CA 92649.

Circle 277 on Inquiry Card

DOUBLE-SIDE FLOPPY DRIVE



With magnetic heads allowing the use of both sides of the medium, the FD200 has an increased storage capacity of 1600k bytes, unformatted. Each head per side is operator selectable. All electronics necessary to perform data transfer operations using only the interface specified control commands are contained. Software interlock to prevent operator error during data transfer operations is optionally available. **General Systems International, Inc,** 1440 Allec St, Anaheim, CA 92805.

Circle 278 on Inquiry Card

MODULAR ILLUMINATED PUSHBUTTON SWITCHES

Low cost, computer grade, illuminated pushbutton switches and matching indicators for panel mounting offer a choice of switch actions and ratings, cap styles and colors, and legends, with uniform mounting dimensions. A common body for all options permits uniform front-of-panel appearance and back-of-panel projection. Part of the 554 series, the devices are designed for single-hole mounting from the rear in panels up to 0.125" (0.3175 cm) thick. Units can be mounted on a sub-panel. **Dialight, a North American Philips Co,** 203 Harrison Pl, Brooklyn, NY 11237.

Circle 279 on Inquiry Card

OCR WAND READER

A hand-held OCR WAND™ reader, Class 600 reads a longer line of alphabetical and numerical characters in structured or random format than the company's previous OCR WAND reader, and can be connected directly to terminals, computers, and other in-house data processing equipment. It optically lifts human-readable source data from a document and transmits them directly to its host device. Intended for OEMs, the device reads and inputs data at speeds of 30 to 130 char/s, with <1 error/10k char scanned. **Recognition Equipment Inc,** PO Box 22307, Dallas, TX 75222.

Circle 280 on Inquiry Card

HVPS your way.

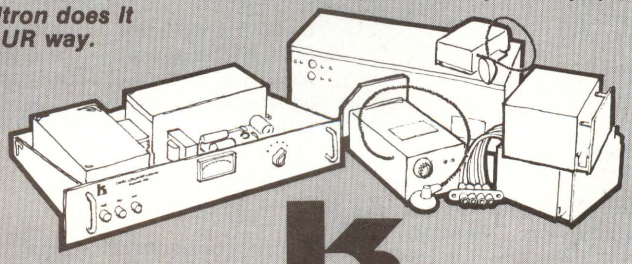
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LITERATURE

Static vs Dynamic Chip Memories

A benchmark study testing the effect of refresh cycle on the CPU performance of an IBM 370/158 reveals results, which indicate advantages of static RAM devices. **Electronic Memories & Magnetics Corp, Computer Products Div,** Hawthorne, Calif.
Circle 300 on Inquiry Card

Switches

Data on company's line of slide, toggle, rocker, rotary, and DIP switches in various sizes and ratings are presented in the form of dimensional diagrams, photos, charts, and descriptions. Highlights include sections on construction and features of each. **CW Industries,** Warminster, Pa.
Circle 301 on Inquiry Card

Digital Switch Patches

Application bulletin provides features and operating information as well as photos and schematic and block diagrams of digital switch patches used in data communications network control. **Spectron Corp,** Mt Laurel, NJ.
Circle 302 on Inquiry Card

Power-Line Disturbance Analyzer

Focusing on applications, features, and theory of operation, bulletin concludes with detailed specs, options, and accessories for second-generation series 606 analyzer. **Dranetz Engineering Laboratories Inc,** South Plainfield, NJ.
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Sockets

Catalog with test data section detailing operating temps, insertion/withdrawal forces, and contact resistance also provides detailed specs and drawings for line of sockets, cables, headers, wirewrap board systems, terminals, and accessories. **Robinson-Nugent, Inc,** New Albany, Ind.
Circle 304 on Inquiry Card

Charge-Transfer Device Technology

Computer Science & Technology: Impact of Charge-Transfer Device Technology on Computer Systems assesses the status, capabilities, and accomplishments of the technology, and compares the technical and economic factors involved. Price of SD Cat No C13.10:500-5 is $1.10. **Superintendent of Documents, U.S. Government Printing Office,** Washington, DC 20402.

Interconnection Components

Photos, schematics, and complete specs for company's panels, terminals, test jacks, and sockets are furnished in product catalog. **Electronic Molding Corp,** Woonsocket, RI.
Circle 305 on Inquiry Card

Multiplexers

Application bulletin with functional block diagrams and schematics is designed to improve user understanding of parameter definitions and measurement techniques for multiplexers. **Teledyne Philbrick,** Dedham, Mass.
Circle 306 on Inquiry Card

Wire/Cable/Cord

An overview of available wire, cable, and cord products, with complete technical information, tables, illustrations, glossary, and a comparison chart, is offered in catalog. **Standard Wire & Cable Co,** El Segundo, Calif.
Circle 307 on Inquiry Card

Programmable Controllers

Detailing the AutoMate 32 programmable controllers with model 31 I/O subsystems, bulletin depicts components and features, and diagrams a typical installation. **Reliance Electric Co,** Cleveland, Ohio.
Circle 308 on Inquiry Card

Voice Numerical Control Programming Systems

Brochure describes advantages of VNC-200 voice programming, listing hardware configurations, options, and basic system vocabulary. **Threshold Technology, Inc,** Delran, NJ.
Circle 309 on Inquiry Card

Solid-State Power Devices

Designer's guide covers applications, basic configurations, features, and key device requirements for solid-state relays, lighting/heater/motor controls, amplifiers, and voltage regulators. **RCA/Solid State Div,** Somerville, NJ.
Circle 310 on Inquiry Card

Microprocessor Modems

Containing photos, standard and optional features, technical data, and operating parameters relevant to the 4800-bit/s modems, brochure also explains remote test capabilities. **International Communications Corp, a Milgo Co,** Miami, Fla.
Circle 311 on Inquiry Card

Smart Multiplexers

Literature package consists of poster, application notes focusing on systems compatible with SMART/MUX family of statistical multiplexers, and illustrated brochure which covers advantages, configurations, and components. **Digital Communications Associates, Inc,** Norcross, Ga.
Circle 312 on Inquiry Card

Sealed Solid-State Keyboards

Illustrated brochure includes mounting dimensions, photos, electrical data, and code and character assignments as well as information on applications and environmental ratings for company's SW-S line of keyboards and sealed key plungers. **Micro Switch, div of Honeywell,** Freeport, Ill.
Circle 313 on Inquiry Card

PCB Connectors

Catalog provides complete specs and schematics for series 1000, 2000, and 3000 Term-Acon® connectors for miniature PCB interconnects, as well as a brief description of bench press and hand crimping tools. **Methode Electronics, Inc,** Rolling Meadows, Ill.
Circle 314 on Inquiry Card

Optoelectronics

Divided into five sections with selection guide and descriptions, comprehensive designer's catalog highlights applications, specs, outline and dimensional drawings, and schematics of lamps, displays, optocouplers, emitters, and PIN photodiodes. **Hewlett-Packard Co, Optoelectronics Div,** Palo Alto, Calif.
Circle 315 on Inquiry Card

Automatic Control

Brochure details videotape series which is designed to provide fundamentals of automatic control by developing principles and operation of control loops, functions of modes, tuning controllers, and applications. **The Foxboro Co,** Foxboro, Mass.
Circle 316 on Inquiry Card

Planar Interconnect Systems

Illustrated with color photos and outline and dimensional drawings, product catalog lists features, characteristics, and applications of company's line of cables, connectors, and assemblies. **Spectra-Strip, an Eltra Co,** Garden Grove, Calif.
Circle 317 on Inquiry Card

Zero Insertion Force Connectors

Basic information including contacts, tooling, applications, shell dimensions, and panel cutouts of rectangular DL series connectors are contained in bulletin with photographs and temp/current graphs. **ITT Corp, Cannon Electric Div,** Santa Ana, Calif.
Circle 318 on Inquiry Card

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